SN93700 Series
HD/FHD Video SoC

1 Introduction

1.1 Features

- ARM926EJ-S
  – Operates up to 402 MHz@1.2V
  – 16 KB instruction cache (I-cache)
  – 16 KB data cache (D-cache)
- 4-channel DMA supports memory-to-memory transfers
- SiP DDR2 32/64 MB up to 402 MHz, 16-bit data bus
- Image Input Interface
  – Supports parallel and single-lane or two-lane MIPI signaling[1]
  – UVC input via USB host
- Image Signal Processing
  – Color processing
  – AE histogram, AWB window, and AF edge window
  – 2D and 3D noise reduction (NR)
  – Wide Dynamic Range (WDR)
  – Digital image stabilization (DIS)
  – Motion detection (MD)
  – Vertical Lens Distortion Correction (vLDC)
  – Machine vision data output
  – Scaling engine
- H.264 Codec
  – I & P picture types
  – Context-based adaptive variable-length code (CAVLC)/ context-adaptive binary arithmetic coding (CABAC) entropy
  – Multi-slice coding
- JPEG Codec
  – Baseline discrete cosine transform (DCT)
  – Two AC, two DC, typical Huffman table at ISO-IEC 10918-1
  – 128 bytes quantization tables for Y and C provide programmable compression ratio
- LCD/TV Interface, resolution up to 1080p
  – 8080 8/9/16-bit data width
  – AUO LCD controller mode
  – AUO UPS051 6/8-bit data width
  – RGB dummy
  – 24-bit data width (DE mode)
  – YUV422 sensor interface
  – BT.656/BT.601
  – CVBS output NTSC/PAL
- Audio Codec
  – 10-bit R2R DAC
  – 16-bit sigma-delta ADC
  – 8K/11.025K/16K/24K/32K/44.1K/48K sampling rate
- I²S
  – 8/16-bit R2R DAC
  – 8/11.025/16/24/32/44.1/48 K sampling rate
  – Full-duplex communication at the same sampling rate
- General Purpose ADC
- RF Interface
  – Up to two sets of RF SPI
  – Supports 2.4 GHz ISM-Band RF transceivers
- 10/100 Mbps Ethernet Media Access Controller (EtherMAC)
  – Fully IEEE 802.3 standard compliant
  – Reduced media independent interface (RMII)
  – Supports flow control for full-duplex and backpressure for half-duplex
- USB 2.0
  – One USB 2.0 host
  – One USB 2.0 host/device option
  – Full-speed and high-speed
- Three sets of three independent 32-bit timers
- Two sets of 32-bit Watchdog Timers (WDT)
- Up to five sets of I²Cs
- Up to 16 pulse width modulator (PWM) outputs to control Iris, IR LED, and status LED
- SPI: Read/write data/command interface compliant with AMBA APB bus 2.0
- Up to two UARTs, wherein one supports flow control (CTS/RTS)
- Up to 21 optional pinmux GPIOs
- Supports boot from SF and UART
- Two crystal oscillators: 32768 Hz and 12 MHz
- Voltage
  – Core: 1.2V typically
  – DRAM: 1.8V typically
  – I/O: 3.3V typically
- Package
  – LQFP128-EP (14 x 14 x 1.4 mm)

[1] Unavailable for SN937x1, x = a variable number

1.2 Description

The SN93700 Series, a multimedia system-on-chip (SoC) solution composed of an ARM926 processor with 16KB I-Cache and 16KB D-Cache as the core. With additional hardware acceleration, the SN93700 Series performs multimedia operations with its video codec, image signal processor (ISP), and audio codec. The H.264 codec supports 30-45 fps @ 1080p[2], 96 fps @ 720p, 25 fps @ (1080p + 720p + 480p) or 25 fps @ (720p + 720p + 720p) multi-streams. The ISP features auto exposure (AE), auto white balance (AWB) control, 2D and 3D noise reduction (NR), wide dynamic range (WDR), and vertical lens distortion correction (vLDC) to allow controls of image presentation. In addition, the ISP provides smart vision features such as digital image stabilizer (DIS), motion detection (MD), and machine vision data output.

The SN93700 Series integrates most of the peripheral interfaces including parallel/MIPI sensor interface[1], USB 2.0 host/device, video output, ADC 4ch, motor controller, and serial flash. It receives CMOS sensor inputs through parallel/MIPI interface and UVC camera inputs through USB 2.0 host interfaces at the same time, and supports video output interfaces for most of the digital LCD panels. For crystal clear audio quality, the noise reduction feature of the SN93700 Series reduces the background noise. The motor controller has two sets of four outputs for stepper motor control used for pan and tilt of the camera motion. For power saving, the ultra-low power mode maximizes operating time of the battery-powered system when a function or interface is disabled.

The software development kit (SDK) of the SN93700 Series includes various sample codes that comply with the Keil® MDK-ARM® compiler. Development, programming and debugging can be implemented efficiently in the Keil MDK-ARM environment.

[2] Unavailable for SN9370x, x = a variable number

1.3 Functional Block Diagram[3]

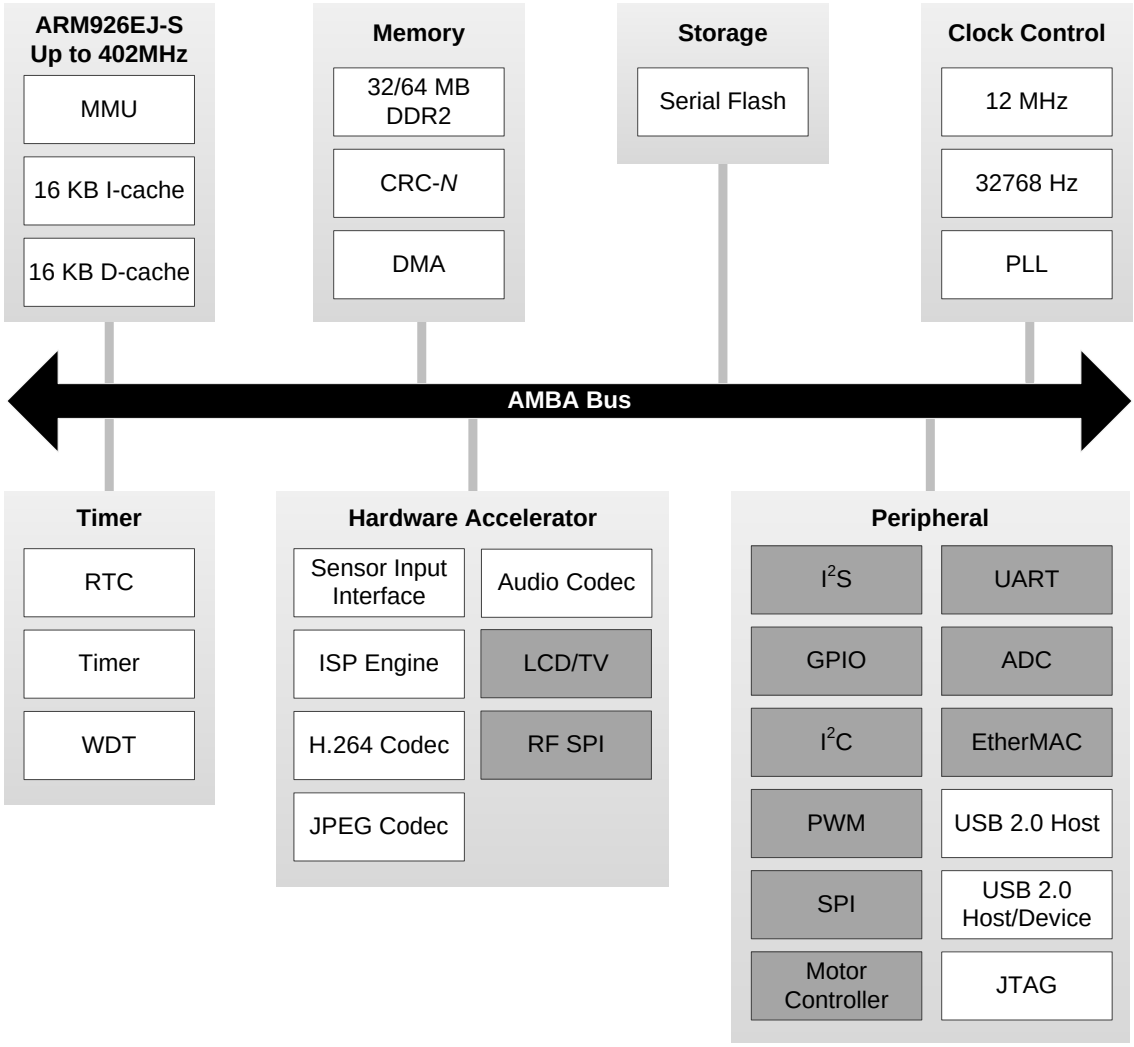


Figure 1–1 Functional Block Diagram

[3] The blocks of functions with pinmux options are shaded.

Revision History

Date	Revision	Description
26-Jun-2018	Preliminary A	Initial release

Convention

WARNING	Indicates a hazard with a medium or low level of risk that, if not avoided, could result in minor or moderate injury.
TIP	Indicates a tip that may help you solve a problem or save time.
NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table of Contents

1 Introduction 1
1.1 Features 1
1.2 Description 2
1.3 Functional Block Diagram 3
2 Device 12
2.1 Specifications 12
2.2 Pin Assignment 15
2.2.1 Pin Map 15
2.2.2 Terminal Functions 17
2.3 Pinmux 23
2.3.1 Pinmux Tables 24
2.3.2 Register Summary 28
2.4 Physical Memory Map 29
2.5 Device Support 32
3 System 33
3.1 ARM Subsystem 33
3.1.1 ARM926EJ-S CPU 33
3.1.2 Memory Management Unit (MMU) 34
3.1.3 Caches 34
3.1.4 CP15 34
3.2 System Controller (Global Settings) 35
3.2.1 Register Summary 35
3.3 Clock Configuration 35
3.3.1 Oscillators 35
3.3.2 Phase-Locked Loops (PLL) 36
3.4 Operating Frequencies 37
3.5 Interrupt Controller (INTC) 37
3.5.1 Interrupt Source Assignment 38
3.5.2 Register Summary 39
3.6 CRC-*N* 39
3.6.1 Register Summary 39
3.7 Direct Memory Access Controller (DMAC) 40
3.7.1 Register Summary 40
3.8 DDR2/DDR SDRAM Memory Controller 41
3.9 Power Management 41
3.10 Boot Mode 41
3.11 Device Reset 44
4 Multimedia 45
4.1 Video 45
4.1.1 Image Input Interface 45
4.1.2 Image Signal Processing (ISP) 47
4.1.3 Video Codecs 49
4.1.4 Image Output Interface (LCD/TV) 53
4.2 Audio 57
4.2.1 I²S Interface 58
4.2.2 Audio Codec 61
4.2.3 Register Summary 62
5 Peripheral and Operating Specifications 64
5.1 General Purpose Input/Output (GPIO) 64
5.1.1 Register Summary 65
5.1.2 Timing 65
5.2 Inter-integrated Circuit (I²C) 66

5.2.1 Register Summary 66
5.2.2 I²C Internal Pinmux 66
5.2.3 Clock Ratios and Timing 67
5.3 Pulse Width Modulator (PWM) 68
5.3.1 Register Summary 69
5.3.2 PWM Pinmux 69
5.3.3 Timing 69
5.4 Serial Peripheral Interface (SPI) 70
5.4.1 Register Summary 70
5.4.2 Clock Ratios and Timing 70
5.5 Universal Asynchronous Receiver Transmitter (UART) 76
5.5.1 Register Summary 77
5.5.2 Baud Rate, Timing, and Transfer Format 77
5.6 Serial Flash (SF) Controller 79
5.6.1 Register Summary 79
5.6.2 Timing 80
5.7 Joint Test Action Group (JTAG) 80
5.7.1 Register Summary 81
5.7.2 Timing 81
5.8 Real Time Clock (RTC) 82
5.8.1 Register Summary 82
5.9 Timer 83
5.9.1 Register Summary 83
5.10 Watchdog Timer (WDT) 83
5.10.1 Register Summary 84
5.11 Ethernet Media Access Controller (EtherMAC) 84
5.11.1 Register Summary 85
5.11.2 Timing 85
5.12 Universal Serial Bus 2.0 (USB 2.0) 87
5.12.1 USB 2.0 Host 88
5.12.2 USB 2.0 Device 90
5.13 Motor Controller (MC) 92
5.13.1 Register Summary 92
5.13.2 Timing 92
5.14 Successive Approximation Register Analog-to-Digital Converter (SAR ADC) 93
5.14.1 Register Summary 93
5.14.2 Timing 93
5.15 RF Serial Peripheral Interface Bus (SPI) 94
6 Device Operating Conditions 95
6.1 Absolute Maximum Ratings 95
6.2 Recommended Operating Conditions 95
6.3 AC Characteristics 96
6.4 Power-up and Power-down Sequence 97
6.4.1 Power-up Sequence 97
6.4.2 Power-down Sequence 97
7 Mechanical Data 98
7.1 Thermal Data 98
7.2 Package Information 98
7.2.1 Nomenclature 98
7.2.2 Package Dimensions 99
7.3 Packaging Appearance and Storage Information 100
7.3.1 Packing Quantity Information 100
7.3.2 Packing Box/Carton Dimension 100
7.3.3 Temperature and Humidity Environmental Control Requirements in Storage 100

7.3.4 Shelf-life 100
Appendix A – The SN93700 Series SDK 101

List of Figures

Figure 1–1 Functional Block Diagram 3
Figure 2–1 SN93700/SN93710 Pin Assignment 15
Figure 2–2 SN93701/SN93711 Pin Assignment 16
Figure 2–3 Pinmux Block Diagram 23
Figure 2–4 Memory Map 30
Figure 3–1 Flow Chart of the Boot Mode Procedure 43
Figure 4–1 Sensor Input Interface 45
Figure 4–2 Sensor Interface SEN_PCLK Timing 46
Figure 4–3 Sensor Interface Slave Mode Input Data Timing 46
Figure 4–4 Input Data Timing in MIPI Master/Slave Mode 47
Figure 4–5 Image Process Flow 48
Figure 4–6 Video Codec Block Diagram 49
Figure 4–7 Video Encoders of the Image Controller 50
Figure 4–8 Image Controller Block Diagram 50
Figure 4–9 JPEG Codec Block Diagram 52
Figure 4–10 LCD Controller Block Diagram 54
Figure 4–11 LCD Layers 54
Figure 4–12 LCD Controller Timing in CPU Mode 56
Figure 4–13 LCD Controller Timing in Non-CPU Mode 57
Figure 4–14 Audio Block Diagram 58
Figure 4–15 I²S Timing 59
Figure 4–16 I²S Transmitter Timing 59
Figure 4–17 I²S Receiver Timing 60
Figure 5–1 GPIO Port Timing 65
Figure 5–2 GPIO External Interrupt 66
Figure 5–3 I²C Receive Timings 68
Figure 5–4 I²C Transmit Timings 68
Figure 5–5 PWM Output Timing 69
Figure 5–6 SPI Connection Diagram 70
Figure 5–7 SPI Master Mode Timings 72
Figure 5–8 SPI Slave Mode Timings 74
Figure 5–9 SPI Master Mode Timing (4-pin) 75
Figure 5–10 SPI Slave Mode Timing (4-pin) 76
Figure 5–11 UART Connection Diagram 77
Figure 5–12 UART Operation Diagram 77
Figure 5–13 UART Transmit/Receive Timing 78
Figure 5–14 UART Transfer Format 78
Figure 5–15 SF Controller Block Diagram 79
Figure 5–16 SF Master Mode Input Timing 80
Figure 5–17 JTAG Input Timing 81
Figure 5–18 JTAG Output Timing 81
Figure 5–19 MAC_TXCLK Timing 85
Figure 5–20 MAC_RXD[1:0], MAC_RX_DV, MAC_RX_ER Timing 86
Figure 5–21 MAC_TXD[1:0], MAC_TX_EN Timing 86
Figure 5–22 MDIO Input Timing 87
Figure 5–23 MAC_MDIO Output Timing 87
Figure 5–24 USB 2.0 Host Integrated Transceiver Interface Timing 89
Figure 5–25 USB 2.0 Device Integrated Transceiver Interface Timing 91
Figure 5–26 Motor Controller Timing 92
Figure 5–27 SAR ADC Channel 0 Timing Diagram 93
Figure 5–28 SAR ADC Single or Multi-Channel Timing 94
Figure 6–1 Power-up Sequence 97

Figure 7–1 Device Nomenclature 98
Figure A1 SDK Structure Based on RTOS for SN93700 Series 101

List of Tables

Table 2–1 Specifications 12
Table 2–2 Sensor Input Interface Pin Description 17
Table 2–3 R2R DAC Pin Description 18
Table 2–4 Sigma-delta ADC Pin Description 18
Table 2–5 Serial Flash Pin Description 19
Table 2–6 RTC Pin Description 19
Table 2–7 IO Pin Description 19
Table 2–8 JTAG Pin Description 20
Table 2–9 MAC Pin Description 21
Table 2–10 USB Pin Description 21
Table 2–11 LCD Pin Description 21
Table 2–12 LCD/TV (CVBS) Pin Description 21
Table 2–13 Misc. Pin Description 22
Table 2–14 Power Pin Description 22
Table 2–15 Function Description of Upper Level Pinmux 24
Table 2–16 Upper Level Pinmux 25
Table 2–17 Internal Level Pinmux 28
Table 2–18 Register of Upper Level Pinmux 28
Table 2–19 Register of Internal Level Pinmux 29
Table 2–20 System Memory Address (REMAP = 0) 31
Table 2–21 System Memory Address (REMAP = 1) 31
Table 2–22 Register Address Ranges 31
Table 3–1 Registers of Global Settings 35
Table 3–2 Oscillators Electrical Requirements and Characteristics 35
Table 3–3 PLL Clock Frequency 36
Table 3–4 PLL List 36
Table 3–5 Maximum Operating Frequencies of CPU, DDR, and Bus 37
Table 3–6 Interrupt Source (IRQ) 38
Table 3–7 Registers of INTC 39
Table 3–8 Registers of CRC-*N* 39
Table 3–9 Registers of DMA Controller 40
Table 3–10 Reset Types 44
Table 4–1 Timing Requirements for SEN_PCLK in Parallel Slave Mode 46
Table 4–2 Timing Requirements for Input Data in Parallel Slave Mode 46
Table 4–3 Timing Requirements for MIPI Master/Slave Mode 47
Table 4–4 Registers of LCD Controller 54
Table 4–5 Switching Characteristics for LCD Controller in CPU Mode 56
Table 4–6 Switching Characteristics for LCD Controller in Non-CPU Mode 57
Table 4–7 Switching Characteristics for I^2S Master Transmitter 60
Table 4–8 Input Timing Requirements for for I^2S Slave Transmitter 60
Table 4–9 Switching Characteristics for I^2S Slave Transmitter 60
Table 4–10 Switching Characteristics for I^2S Master Receiver 61
Table 4–11 Input Timing Requirements for for I^2S Master Receiver 61
Table 4–12 Input Timing Requirements for I^2S Slave Receiver 61
Table 4–13 Registers of Audio Codec 62
Table 5–1 List of GPIOs 64
Table 5–2 Registers of GPIO 65
Table 5–3 Switching Characteristics for GPIO Outputs 65
Table 5–4 Registers of I^2C 66
Table 5–5 Timing Requirements for I²C 67
Table 5–6 Switching Characteristics for I²C 68
Table 5–7 Registers of PWM 69

Table 5–8 Switching Characteristics for PWM Outputs 69
Table 5–9 Registers of SPI 70
Table 5–10 Switching Characteristics for SPI in Master Mode 73
Table 5–11 Input Timing Requirements for SPI in Master Mode 73
Table 5–12 Switching Characteristics for SPI in Slave Mode 75
Table 5–13 Input Timing Requirements for SPI in Slave Mode 75
Table 5–14 Output Switching Characteristics of 4-pin Chip-select Option in Master Mode 75
Table 5–15 Output Switching Characteristics of 4-pin Chip-select Option in Slave Mode 76
Table 5–16 Additional Input Timing Requirements of 4-pin Chip-select Option in Slave Mode 76
Table 5–17 Registers of UART 77
Table 5–18 Timing Requirements for UART Receiver 78
Table 5–19 Switching Characteristics for UART Transmitter 78
Table 5–20 Registers of Serial Flash 79
Table 5–21 Switching Characteristics for SF Controller 80
Table 5–22 Input Timing Requirements of SF Controller in Master Mode 80
Table 5–23 Timing Requirements for JTAG Test Port 81
Table 5–24 Switching Characteristics for JTAG Test Port 82
Table 5–25 Registers of RTC 82
Table 5–26 Registers of Timer 83
Table 5–27 Registers of WDT 84
Table 5–28 Registers of EtherMAC 85
Table 5–29 Timing Requirements for MAC_TXCLK 85
Table 5–30 Timing Requirements for MAC_RXD[1:0], MAC_RX_DV, and MAC_RX_ER 86
Table 5–31 Switching Characteristics for MAC_TXD[1:0] and MAC_TX_EN 86
Table 5–32 Timing Requirements for Management Data Input/Output (MAC_MDIO) 87
Table 5–33 Switching Characteristics for MAC_MDIO Output 87
Table 5–34 Register Summary of USB 2.0 Host 89
Table 5–35 Switching Characteristics for USB 2.0 Host 90
Table 5–36 Register Summary of USB 2.0 Device 91
Table 5–37 Switching Characteristics for USB 2.0 Device 91
Table 5–38 Register Summary of Motor Controller 92
Table 5–39 Switching Characteristics for MC Outputs 93
Table 5–40 Registers of SAR ADC 93
Table 5–41 Switching Characteristics for SAR ADC 94
Table 6–1 Absolute Maximum Ratings 95
Table 6–2 Recommended Operating Conditions 95
Table 6–3 Electrical Characteristics over Recommended Ranges 96
Table 6–4 AC Value Summary 96
Table 7–1 Packing Quantity Information 100
Table 7–2 Packing Box/Carton Dimension 100
Table 7–3 Store Condition 100

2 Device

2.1 Specifications
2.2 Pin Assignment
2.3 Pinmux
2.4 Physical Memory Map
2.5 Device Support

2.1 Specifications

Table 2–1 Specifications

System	
CPU	ARM926EJ-S processor 402 MHz@1.2V with 16 KB I-cache, and 16 KB D-cache
Chip Frequency	12 MHz and 32768 Hz crystal AMBA AXI • bus0: Up to 268.00 MHz • bus1: Up to 324.00 MHz • bus2: Up to 268.00 MHz • bus3: Up to 324.00 MHz AMBA AHB • bus0: Up to 201.00 MHz • bus1: Up to 120.00 MHz • bus2: Up to 96.00 MHz • bus3: Up to 268.00 MHz AMBA APB bus: Up to 48.00 MHz
CRC-*N*	CRC-*N* MOD codec
DMA Controller	Four channels that support memory-to-memory transfers
DDR Controller	Supports SiP DDR2 32/64 MB up to 402 MHz, 16-bit data bus
Boot	Supports boot from SF and UART
Multimedia	
Image Input Interface	Parallel data input; 10-bits RAW and YUV4:2:2[1] MIPI CSI-2[1] up to 804 Mbps with dual data lane x2 or single data lane x4 that supports up to four video channel inputs Two UVC cam inputs connected via the USB hosts
Sensor Resolution and Format	Super HD (2304 x 1296)[4], QXGA (2048 x 1536), UXGA (1600 x 1200), 1080P (1920 x 1080), SXGA (1280 x 1024), 720P (1280 x 720)[5], VGA (640 x 480) with CMOS ISP/Bayer RAW sensors
Image Signal Processing (ISP)	Supports AE/AWB/AF/2DNR/3DNR/WDR/DIS/MD/vLDC and alpha-blending OSD in four-color text mode Color processing Machine vision data output Scaling engine
Video Codec	H.264 BP/MP/HP Level 4.1 codec, baseline JPEG encoder and baseline JPEG codec Rate control supporting auto region of interest (AROI) or manual region of interest (MROI) for eight regions Flexible multi-streaming H.264 codec • I & P picture types • Context-based adaptive variable-length code (CAVLC)/context-adaptive binary arithmetic coding (CABAC) entropy • Multi-slice coding

[4] Only SN93710 supports up to Super HD.
[5] Up to 720P for SN93700

Multimedia	
Video Codec	JPEG codec • Baseline discrete cosine transform (DCT) • Fixed Huffman table (two AC, two DC, typical Huffman table at ISO-IEC 10918-1) • 128 bytes quantization tables for Y and C provide programmable compression ratio 256-color graphic mode OSD for image merging
LCD/TV Interface	Data enable mode 24-bit data width[6] CPU 8080 8/9[6]/16[6]-bit data width • 8-bit data width, 2 bytes/pixel, RGB565 • 8-bit data width, 3 bytes/pixel, RGB888 • 9-bit data width, 2 bytes/pixel, RGB666[6] • 16-bit data width, RGB565[6] AUO LCD controller mode AUO UPS051 6/8-bit data width RGB dummy UPS051, UPS052, AT3210, ST7528, IST3101 YUV422 sensor interface BT.656/BT.601 CVBS output: NTSC/PAL 256-color graphic mode OSD
LCD Resolution	Up to 1920 x 1080 @60 fps[7]
Audio Codec	16-bit sigma-delta ADC and 10-bit R2R DAC 8K/11.025K/16K/24K/32K/44.1K/48K sampling rate
ADC	10-bit, up to four channels Pinmux options as GPIO
I²S	8/16-bit resolution 8K/11.025K/16K/24K/32K/44.1K/48K sampling rate Full-duplex communication at the same sampling rate
Peripheral	
GPIO	Up to 21 pins with pinmux options Each GPIO port triggers the GPIO interrupt separately De-bounce function for each GPIO
I²C	Up to five sets Up to 100 KHz and up to 400 KHz in fast-mode 7-bit, 10-bit, and general call addressing modes Slave mode general call address detection
PWM	Up to 16 pins with pinmux options PWM outputs to control Iris, IR LED, and status LED
SPI	One set Read/write data/command interface compliant with AMBA APB bus 2.0
UART	Up to two sets, baud rates: 9600, 19200, 38400, 51200, 115200 and up to 12 Mbps Flow control (CTS/RTS) feature
Serial Flash	One set serial flash controller with CRC-32/16
JTAG	One set for device emulation
Real Time Clock	30-bit timer 30-bit alarm timer 24-bit wakeup timer
Timer	Three sets of three independent 32-bit timer programming models Interrupts issued upon the overflow and time-up Programmable decrementing/incrementing modes
Watchdog Timer	Two sets 32-bit watchdog counter Built-in a 32 KHz ILRC

[6] Unavailable for SN937x0, x = a variable number
[7] SN93711 and SN93721: Up to 1080P (1920 x 1080) @60 fps
SN93701: Up to 720P (1280 x 720) @60 fps
SN93700 and SN93710: Up to 480P (800 x 480) @60 fps

Peripheral	
Ethernet	Up to one 10/100 Mbps EtherMAC with RMII interface Fully IEEE 802.3 standard compliant Supports flow control for full-duplex and backpressure for half-duplex
USB	One USB 2.0 high speed host controller, and one USB 2.0 high speed host/device option, forward compatible with full-speed mode
RF Interface	Up to two sets of RF SPI Firmware protocol base adaptive Frequency-hopping Spreading Spectrum (FHSS) Firmware protocol for anti-interference algorithm Supports ID paring for security One-way video, two-way audio and two-way command Supports 2.4 GHz ISM-Band RF transceivers including AMICCOM A7121 (3 Mbps), AMICCOM A7130 (4 Mbps) and AMICCOM A7196 (6 Mbps)
Motor Controller	Up to two sets of four output signals for stepper motor control
Mechanical Data	
Voltage	Core: 1.14V to 1.26V (1.2V typical) DRAM: 1.7V to 1.9V (1.8V typical) I/O: 3.0V to 3.6V (3.3V typical)
Package	LQFP128-EP (14 x 14 x 1.4 mm)

2.2 Pin Assignment

2.2.1 Pin Map

Two pin types are available for the SN93700 Series. Figure 2–1 and Figure 2–2 are the pin assignments of LQFP128-TX and RX. For detailed pin information, refer to subsection 2.2.2.

I. SN93700/SN93710 Pin Assignment

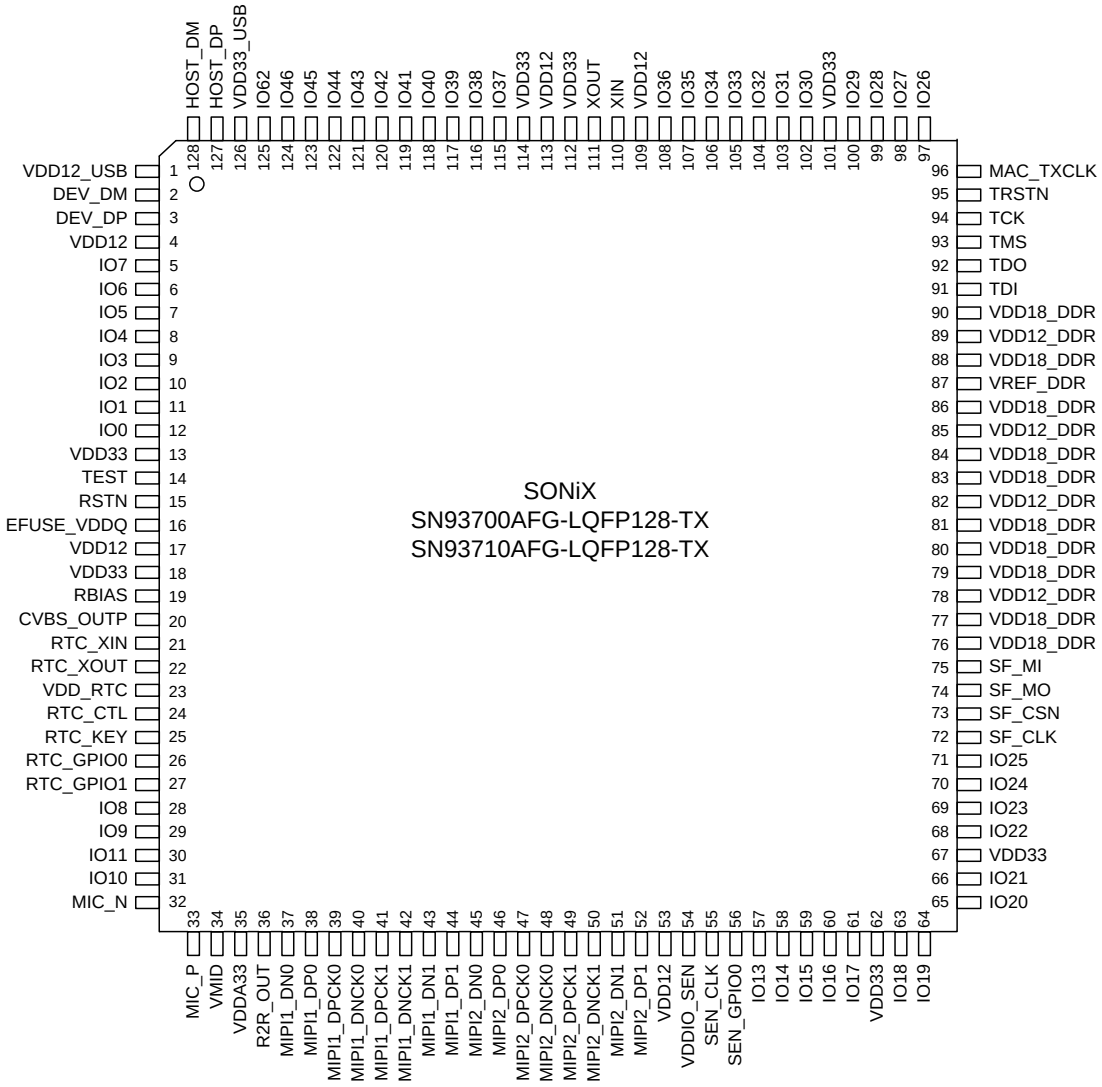


Figure 2–1 SN93700/SN93710 Pin Assignment

II. SN93701/SN93711 Pin Assignment

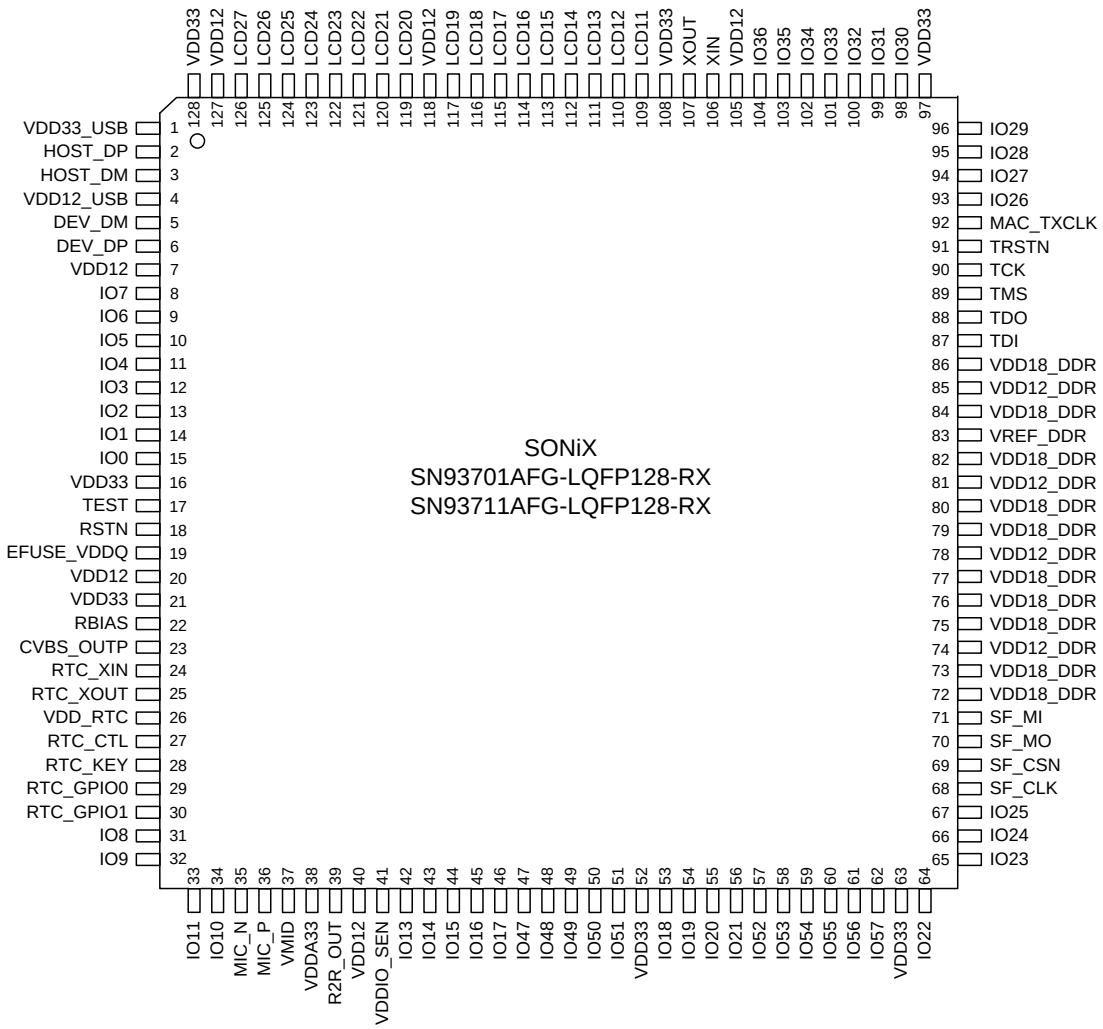


Figure 2–2 SN93701/SN93711 Pin Assignment

2.2.2 Terminal Functions

Table 2–2 Sensor Input Interface Pin Description

Pinmux: Non-multiplexed

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
MIPI1_DN0/ SEN_VSYNC[10]	37	–	I	MIPI 1 lane 0 differential data input, negative/ Parallel image sensor VSYNC input; • Power supply: VDDIO_SEN • PU/PD: PD
MIPI1_DP0/ SEN_PCLK[10]	38	–	I	MIPI 1 lane 0 differential data input, positive/ Parallel image sensor pixel clock input; • Power supply: VDDIO_SEN • PU/PD: PD
MIPI1_DPCK0/ SEN_HSYNC[10]	39	–	I	MIPI 1 lane 0 differential clock input, positive/ Parallel image sensor HSYNC input; • Power supply: VDDIO_SEN • PU/PD: PD
MIPI1_DNCK0/ SEN_D0	40	–	I	MIPI 1 lane 0 differential clock input, negative/ Parallel image sensor data input; • Power supply: VDDIO_SEN • PU/PD: PD
MIPI1_DPCK1/ SEN_D1	41	–	I	MIPI 1 lane 1 differential clock input, positive/ Parallel image sensor data input; • Power supply: VDDIO_SEN • PU/PD: PD
MIPI1_DNCK1/ SEN_D2	42	–	I	MIPI 1 lane 1 differential clock input, negative/ Parallel image sensor data input; • Power supply: VDDIO_SEN • PU/PD: PD
MIPI1_DN1/ SEN_D4	43	–	I	MIPI 1 lane 1 differential data input, negative/ Parallel image sensor data input; • Power supply: VDDIO_SEN • PU/PD: PD
MIPI1_DP1/ SEN_D3[10]	44	–	I	MIPI 1 lane 1 differential data input, positive/ Parallel image sensor data input; • Power supply: VDDIO_SEN • PU/PD: PD
MIPI2_DN0/ SEN_D6[10]	45	–	I	MIPI 2 lane 0 differential data input, negative/ Parallel image sensor data input; • Power supply: VDDIO_SEN • PU/PD: PD
MIPI2_DP0/ SEN_D5[10]	46	–	I	MIPI 2 lane 0 differential data input, positive/ Parallel image sensor data input; • Power supply: VDDIO_SEN • PU/PD: PD
MIPI2_DPCK0/ SEN_D7[10]	47	–	I	MIPI 2 lane 0 differential clock input, positive/ Parallel image sensor data input; • Power supply: VDDIO_SEN • PU/PD: PD

[8] Signal Types:
I = Input
O = Output
A = Analog signal
P = Power
GND = Ground

[9] Abbreviations:
PU: Pull-up. A resistor to make sure that the signal maintains stable high when no device is actively driving the net
PD: Pull-down. A resistor to make sure that the signal maintains stable low when no device is actively driving the net.
DS: Drive strength

[10] When SEN_PULL_DOWN is set to 1, the direction turns to be output and outputs low.

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
MIPI2_DNCK0/ SEN_D8[10]	48	–	I	MIPI 2 lane 0 differential clock input, negative/ Parallel image sensor data input; • Power supply: VDDIO_SEN • PU/PD: PD
MIPI2_DPCK1/ SEN_D9[10]	49	–	I	MIPI 2 lane 1 differential clock input, positive/ Parallel image sensor data input; • Power supply: VDDIO_SEN • PU/PD: PD
MIPI2_DNCK1	50	–	I	MIPI 2 lane 1 differential clock input, negative • Power supply: VDDIO_SEN • PU/PD: PD
MIPI2_DN1	51	–	I	MIPI 2 lane 1 differential data input, negative • Power supply: VDDIO_SEN • PU/PD: PD
MIPI2_DP1	52	–	I	MIPI 2 lane 1 differential data input, positive • Power supply: VDDIO_SEN • PU/PD: PD
SEN_CLK	55	–	O	Parallel image sensor master clock output • DS: 12 mA • Power supply: VDDIO_SEN • PU/PD: –
SEN_GPIO0	56	–	I/O	GPIO0 for sensor controlling • DS: 8 mA • Power supply: VDDIO_SEN • PU/PD: PD

Table 2–3 R2R DAC Pin Description

Pinmux: Non-multiplexed

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
R2R_OUT	36	39	O	R2R DAC output • Power supply: DAC_VDDA • PU/PD: PD

Table 2–4 Sigma-delta ADC Pin Description

Pinmux: Non-multiplexed

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
VMID	34	37	I/O	Middle reference voltage, connected to bypass capacitors • Power supply: VDDA33 x 0.5 • PU/PD: –
MIC_N	32	35	I	Microphone differential negative input • Power supply: VDDA33 • PU/PD: –
MIC_P	33	36	I	Microphone single-end positive input • Power supply: VDDA33 • PU/PD: –

Table 2–5 Serial Flash Pin Description

Pinmux: Non-multiplexed

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
SF_CLK	72	68	O	Serial flash clock output • Power supply: VDD33 • DS: 12 mA • PU/PD: PU
SF_CSN	73	69	O	Serial flash chip select, active low; • Power supply: VDD33 • DS: 8 mA • PU/PD: PU
SF_MO	74	70	O	Serial flash data output • Power supply: VDD33 • DS: 8 mA • PU/PD: PU
SF_MI	75	71	I	Serial flash data input • Power supply: VDD33 • DS: 8 mA • PU/PD: PU

Table 2–6 RTC Pin Description

Pinmux: Non-multiplexed

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
RTC_XIN	21	24	I	RTC 32768 Hz crystal input • Power supply: VDD_RTC • PU/PD: –
RTC_XOUT	22	25	O	RTC 32768 Hz crystal output • Power supply: VDD_RTC • PU/PD: –
RTC_CTL	24	27	O	RTC control output • Power supply: VDD_RTC • PU/PD: –
RTC_KEY	25	28	I	RTC input, wakeup • Power supply: VDD_RTC • PU/PD: –
RTC_GPIO0	26	29	I/O	RTC GPIO pin 0, wakeup • Power supply: VDD_RTC • PU/PD: –
RTC_GPIO1	27	30	I/O	RTC GPIO pin 1, wakeup • Power supply: VDD_RTC • PU/PD: –

Table 2–7 IO Pin Description

Pinmux: See **Table 2–16**

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
IO[7:0]	5–12	8–15	I/O	Upper level pinmux input/output 7 to 0 • DS: 8 mA • Power supply: VDD33 • PU/PD: PU
IO[11:8]	30, 31, 29, 28	33, 34, 32, 31	I/O	Upper level pinmux input/output 11 to 8 Alternatively 10-bit SAR ADC input CH3 to CH0 • DS: 16 mA • Power supply: VDD33 • PU/PD: PD

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
IO[17:13]	61–57	46–42	I/O	Upper level pinmux input/output 17 to 13 • DS: 8 mA • Power supply: VDDIO_SEN • PU/PD: PD
IO[25:18]	71–68, 66–63	67–64, 56–53	I/O	Upper level pinmux input/output 25 to 18 • DS: 8 mA • Power supply: VDD33 • PU/PD: PU
IO[36:26]	108–102, 100–97	104–98, 96–93	I/O	Upper level pinmux input/output 36 to 26 • DS: 12 mA • Power supply: VDD33 • PU/PD: PU
IO[46:37]	124–115	–	I/O	Upper level pinmux input/output 46 to 37 • DS: 8 mA • Power supply: VDD33 • PU/PD: PU
IO[57:47]	–	62–57, 51–47	I/O	Upper level pinmux input/output 57 to 47 • DS: 8 mA • Power supply: VDD33 • PU/PD: PU
IO62	125	–	I/O	Upper level pinmux input/output 62 • DS: 8 mA • Power supply: VDD33 • PU/PD: PU

Table 2–8 JTAG Pin Description

Pinmux: See Table 2–17

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
TDI	91	87	I	JTAG test data in or GPIO • DS: 8 mA • Power supply: VDD33 • PU/PD: PU
TDO	92	88	O	JTAG test data out or GPIO • DS: 8 mA • Power supply: VDD33 • PU/PD: PU
TMS	93	89	I	JTAG test mode select or GPIO • DS: 8 mA • Power supply: VDD33 • PU/PD: PU
TCK	94	90	I	JTAG test clock or GPIO • DS: 8 mA • Power supply: VDD33 • PU/PD: PU
TRSTN	95	91	I	JTAG test reset, active low, or GPIO • DS: 8 mA • Power supply: VDD33 • PU/PD: PU

Table 2–9 MAC Pin Description[11]

Pinmux: Non-multiplexed

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
MAC_TXCLK	96	92	O	Reference clock • DS: 8 mA • Power supply: VDD33 • PU/PD: –

Table 2–10 USB Pin Description

Pinmux: Non-multiplexed

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
HOST_DM	128	3	A I/O	USB D- signal; carries USB data to and from the USB 2.0 PHY • DS: 8 mA • Power supply: – • PU/PD: –
HOST_DP	127	2	A I/O	USB D+ signal; carries USB data to and from the USB 2.0 PHY • DS: 8 mA • Power supply: – • PU/PD: –
DEV_DM	2	5	A I/O	USB D- signal; carries USB data to and from the USB 2.0 PHY • Power supply: – • PU/PD: –
DEV_DP	3	6	A I/O	USB D+ signal; carries USB data to and from the USB 2.0 PHY • Power supply: – • PU/PD: –

Table 2–11 LCD Pin Description[12]

Pinmux: See Table 2–17

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
LCD[19:11]	–	117–109	I/O	LCD control output or GPIO • DS: 12 mA • Power supply: VDD33 • PU/PD: –
LCD[27:20]	–	126–119	I/O	LCD control output or GPIO • DS: 12 mA • Power supply: VDD33 • PU/PD: –

Table 2–12 LCD/TV (CVBS) Pin Description

Pinmux: Non-multiplexed

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
RBIAS	19	22	I/O	Video DAC current biasing • Power supply: – • PU/PD: –

[11] The MAC interface has 12 pins: 11 pins of upper level pinmux and the pin listed in Table 2–9.
[12] The LCD interface has 28 pins: 11 pins of upper level pinmux and the 17 pins listed in Table 2–11.

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
CVBS_OUTP	20	23	O	Video DAC positive output • Power supply: – • PU/PD: –

Table 2–13 Misc. Pin Description

Pinmux: Non-multiplexed

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
RSTN	15	18	I	Hardware reset, active low • Power supply: VDD33 • PU/PD: PD
TEST	14	17	I	Test mode select, always tie low • Power supply: VDD33 • PU/PD: –
XIN	110	106	I	12 MHz crystal input • Power supply: VDD33 • PU/PD: –
XOUT	111	107	O	12 MHz crystal output • Power supply: VDD33 • PU/PD: –

Table 2–14 Power Pin Description

Pinmux: Non-multiplexed

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
VDD12	4, 17, 53, 109, 113	7, 20, 40, 105, 118, 127	P	Digital core power • Power supply: 1.2V • PU/PD: –
VDD33	13, 18, 62, 67, 101, 112, 114	16, 21, 52, 63, 97, 108, 128	P	I/O power • Power supply: 3.3V • PU/PD: –
VDD12_USB	1	4	P	USB host/device power • Power supply: 1.2V • PU/PD: –
VDD33_USB	126	1	P	USB host/device power • Power supply: 3.3V • PU/PD: –
VDDIO_SEN	54	41	P	MIPI/Parallel sensor interface I/O power Can be 1.8V to 3.3V depending on the sensor I/O voltage level. • Power supply: 1.8V to 3.3V • PU/PD: –
EFUSE_VDDQ	16	19	P	E-fuse program power Tie ground for the chip to function normally • Power supply: 0V in the normal mode or 2.5V in the program mode. • PU/PD: –
VDD_RTC	23	26	P	RTC power • Power supply: 1.4V to 3.6V • PU/PD: –
VDDA33	35	38	P	Sigma-delta ADC, SAR, ADC, 10-bit R2R DAC, MIPI power • Power supply: 3.3V • PU/PD: –

Name	Pin No.		Type[8]	Description[9]
	TX	RX		
VDD18_DDR	76, 77, 79–81, 83, 84, 86, 88, 90	72, 73, 75–77, 79, 80, 82, 84, 86	P	Post-driver power in DDR2 I/O domain • Power supply: 1.8V • PU/PD: –
VDD12_DDR	78, 82, 85, 89	74, 78, 81, 85	P	Core power in DDR2 I/O domain • Power supply: 1.2V • PU/PD: –
VREF_DDR	87	83	P	DDR2 I/O receiver reference voltage • Power supply: 0.9V • PU/PD: –
Thermo pad (VSS)	–	–	GND	I/O or digital core ground • Power supply: 0V • PU/PD: –

2.3 Pinmux

Extensive use of pin multiplexing (pinmux) allows reusing the same pin for different purposes. Pinmux is controlled by a combination of hardware configuration at device reset and software programmable register settings.

The SN93700 Series has two pinmux levels, one upper level for peripheral multiplexing and one internal level for alternate selection of each peripheral. Each upper level peripheral multiplexing I/O pin can be controlled individually as a user controllable GPIO pin or an internal connection to one of the peripherals (e.g., I²C). The internal level pinmux serves its own function or as GPIO. When a pin is configured as GPIO mode, the peripherals connected to it are disabled.

Interrupt mode is supported in upper level pinmux GPIO. When the upper level pinmux GPIO module is selected, there is an IRQ connected between the IP and INTC. Modes and data must all be programmed and then poll for the status of each upper level pinmux GPIO pin when a pin is set to the GPIO input mode.

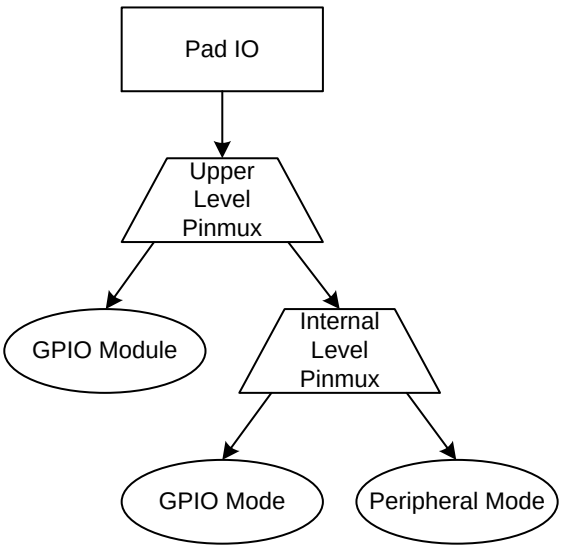


Figure 2–3 Pinmux Block Diagram

2.3.1 Pinmux Tables

Pin multiplexing allows I/O pins to be set as a pin of another function. Table 2–15 to Table 2–17 show complete lists of pins of upper level pinmux and internal level pinmux.

Table 2–15 Function Description of Upper Level Pinmux

Function	Name	Type[13]	Description
GPIO	GPIO[13:0]	I/O	General purpose input output
I²S	I2S_DATA_IN	I	I²S data input or GPIO
	I2S_DATA_OUT	O	I²S data output or GPIO
	I2S_BCLK	I/O	I²S bit clock or GPIO. Bit clock can be programmed as a master or a slave.
	I2S_MCLK	I/O	I²S master clock or GPIO. Master clock can be generated from an external clock source or be an internal generated clock.
	I2S_LRCK	I/O	I²S L/R clock or GPIO. L/R clock can be programmed as a master or a slave.
I²C 1	I2C1_SCL	O	I²C 1 serial clock or GPIO
	I2C1_SDA	I/O	I²C 1 serial data or GPIO
I²C 2	I2C2_SCL	O	I²C 2 serial clock or GPIO
	I2C2_SDA[3:0]	I/O	I²C 2 serial data or GPIO
PWM	PWM[15:0]	O	Pulse width modulation data output
SPI	SPI_CLK	O	SPI serial clock or GPIO
	SPI_CSN	O	SPI chip select, active low or GPIO
	SPI_MO	O	SPI master data output or GPIO
	SPI_MI	I	SPI master data input or GPIO
UART 1	UART1_TX	O	UART 1 serial data output or GPIO
	UART1_RX	I	UART 1 serial data input or GPIO
UART 2	UART2_TX	O	UART 2 serial data output or GPIO
	UART2_RX	I	UART 2 serial data input or GPIO
	UART2_CTS	I	UART 2 flow control input or GPIO, clear to send
	UART2_RTS	O	UART 2 flow control output or GPIO, request to send
MAC	MAC_TX_EN	O	RMII transmit enable
	MAC_TXD[1:0]	O	RMII transmit data
	MAC_RX_DV	I	RMII carrier sense/receive data valid
	MAC_RX_ER	I	RMII receive error input
	MAC_RXD[1:0]	I	RMII receive data
	MAC_MDC	O	RMII management control interface clock
	MAC_MDIO	I/O	RMII management control interface data
	MAC_PHY_LINKSTS	I	MAC PHY link status
	MAC_PDN_PHY	O	Signal to power down MAC PHY
MC 0	MC0_[3:0]	O	Motor control 0 output
MC 1	MC1_[3:0]	O	Motor control 1 output
LCD	LCD[10:0]	I/O	LCD control output or GPIO
RF1_SPI	RF1_SPI_CLK	O	SPI serial clock for RF 1 control
	RF1_SPI_CSN	O	SPI chip select for RF 1 control, active low
	RF1_SPI_MO	O	SPI master data out for RF 1 control
	RF1_SPI_MI	I	SPI master data in for RF 1 control
RF2_SPI	RF2_SPI_CLK	O	SPI serial clock for RF 2 control
	RF2_SPI_CSN	O	SPI chip select for RF 2 control, active low
	RF2_SPI_MO	O	SPI master data out for RF 2 control
	RF2_SPI_MI	I	SPI master data in for RF 2 control
RF_CTRL	RF1_CTRL[2:0]	I/O	Control pin 2 to 0 for RF 1 control
	RF2_CTRL[2:0]	I/O	Control pin 2 to 0 for RF 2 control
SAR ADC	AIN[5:1]	I	ADC input channel 5 to 1

[13] The types listed below represent pin type of the primary function. For pins with GPIO as pinmux option, the pin type is I/O when being used as GPIO.

Table 2–16 Upper Level Pinmux

Pin Name	Mode 0[14]	Mode 1	Mode 2	Mode 3[15]	Mode 4	Mode 5[15]	Mode 6[15]	Mode 7	Note[15]
IO0	GPIO0	MC0_0	I2C1_SCL	–	–	–	–	PWM0	–
IO1	GPIO1	MC0_1	I2C1_SDA	–	–	–	–	PWM1	–
IO2	GPIO2	MC0_2	UART1_TX	–	–	–	–	PWM2	–
IO3	GPIO3	MC0_3	UART1_RX	–	–	–	–	PWM3	–
IO4	GPIO4	MC1_0	UART2_TX	–	–	–	–	PWM4	–
IO5	GPIO5	MC1_1	UART2_RX	–	–	–	–	PWM5	–
IO6	GPIO6	MC1_2	UART2_CTS	–	–	I2C1_SCL	–	PWM6	–
IO7	GPIO7	MC1_3	UART2_RTS	–	–	I2C1_SDA	–	PWM7	–
IO8	GPIO8	UART2_TX	SPI_MI	–	I2S_MCLK	RF1_CTRL0	–	PWM8	AIN1[16]
IO9	GPIO9	UART2_RX	SPI_CSN	–	I2S_BCLK	MC0_0	–	PWM9	AIN2[16]
IO10	GPIO10	UART2_CTS	SPI_CLK	–	I2S_LRCK	MC0_1	–	PWM10	AIN3[16]
IO11	GPIO11	UART2_RTS	SPI_MO	–	I2S_DATA_OUT	MC0_2	–	PWM11	AIN4[16]
IO12	GPIO12	I2C1_SDA	RF1_CTRL1	–	I2S_DATA_IN	MC0_3	–	PWM12	AIN5[16]
IO13	GPIO13	UART2_TX	I2S_MCLK	–	I2C2_SCL	MC1_0	–	PWM13	Variable voltage[17]
IO14	GPIO0	UART2_RX	I2S_BCLK	–	I2C2_SDA0	MC1_1	–	PWM14	Variable voltage
IO15	GPIO1	UART1_RX	I2S_LRCK	MAC_TX_EN	I2C2_SDA1	MC1_2	–	PWM15	Variable voltage
IO16	GPIO2	UART1_TX	I2S_DATAIN	MAC_TXD0	I2C2_SDA2	MC1_3	–	PWM0	Variable voltage
IO17	GPIO3	RF1_CTRL2	I2S_DATAOUT	MAC_TXD1	I2C2_SDA3	RF2_CTRL0	–	PWM1	Variable voltage
IO18	GPIO4	RF1_SPI_CLK	SPI_CLK	MAC_RX_DV	–	I2S_MCLK	–	PWM2	–
IO19	GPIO5	RF1_SPI_CSN	SPI_CSN	MAC_RX_ER	–	I2S_BCLK	–	PWM3	–
IO20	GPIO6	RF1_SPI_MO	SPI_MO	MAC_RXD0	–	I2S_LRCK	–	PWM4	–
IO21	GPIO7	RF1_SPI_MI	SPI_MI	MAC_RXD1	–	I2S_DATA_IN	–	PWM5	–
IO22	GPIO8	RF2_SPI_MO	UART2_TX	MAC_MDC	–	I2S_DATA_OUT	–	PWM6	–
IO23	GPIO9	RF2_SPI_MI	UART2_RX	MAC_MDIO	–	I2C1_SCL	–	PWM7	–
IO24	GPIO10	RF2_SPI_CLK	UART2_CTS	MAC_PHY_LINKSTS	–	I2C1_SDA	–	PWM8	–

[14] When using a specific GPIO by setting two or more IO pins, there is a priority in GPIO input mode. The lower order number of IO pin has higher priority to be configured as input, so the others must set to other pinmux mode.
[15] The "–"s represent reserved pinmux options.
[16] These IO pins can be configured as ADC input pins by setting the SAR ADC internal register.
[17] The voltage of these pins is 1.8V or 3.3V complying with the voltage of VDDIO_SEN.

Pin Name	Mode 0[14]	Mode 1	Mode 2	Mode 3[15]	Mode 4	Mode 5[15]	Mode 6[15]	Mode 7	Note[15]
IO25	GPIO11	RF2_SPI_CSN	UART2_RTS	MAC_PDN_PHY	–	RF2_CTRL1	–	PWM9	–
IO26	GPIO12	RF1_CTRL0	–	–	MAC_TX_EN	LCD0	–	PWM10	–
IO27	GPIO13	RF1_CTRL1	–	–	MAC_TXD0	LCD1	–	PWM11	–
IO28	GPIO0	RF1_CTRL2	–	–	MAC_TXD1	LCD2	–	PWM12	–
IO29	GPIO1	RF2_CTRL0	–	–	MAC_RX_DV	LCD3	–	PWM13	–
IO30	GPIO2	RF2_CTRL1	–	–	MAC_RX_ER	LCD4	–	PWM14	–
IO31	GPIO3	RF2_CTRL2	–	–	MAC_RXD0	LCD5	–	PWM15	–
IO32	GPIO4	RF2_CTRL2	I2S_MCLK	–	MAC_RXD1	LCD6	–	PWM0	–
IO33	GPIO5	SPI_CLK	I2S_BCLK	–	MAC_MDC	LCD7	–	PWM1	–
IO34	GPIO6	SPI_CSN	I2S_LRCK	–	MAC_MDIO	LCD8	–	PWM2	–
IO35	GPIO7	SPI_MO	I2S_DATA_OUT	–	MAC_PHY_LINKSTS	LCD9	–	PWM3	–
IO36	GPIO8	SPI_MI	I2S_DATA_IN	–	MAC_PDN_PHY	LCD10	–	PWM4	–
IO37	GPIO9	–	I2C1_SCL	–	SPI_CLK	UART1_TX	–	PWM5	–
IO38	GPIO10	–	I2C1_SDA	–	SPI_CSN	UART1_RX	–	PWM6	–
IO39	GPIO11	–	RF1_SPI_CLK	–	SPI_MO	MC0_0	–	PWM7	–
IO40	GPIO12	–	RF1_SPI_MI	–	SPI_MI	MC0_1	–	PWM8	–
IO41	GPIO13	–	RF1_SPI_MO	–	I2C1_SCL	MC0_2	–	PWM9	–
IO42	GPIO0	–	RF1_SPI_CSN	–	I2C1_SDA	MC0_3	–	PWM10	–
IO43	GPIO1	–	RF2_SPI_CSN	–	UART1_TX	MC1_0	–	PWM11	–
IO44	GPIO2	–	RF2_SPI_CLK	–	UART1_RX	MC1_1	–	PWM12	–
IO45	GPIO3	I2C1_SCL	RF2_SPI_MO	–	UART2_TX	MC1_2	–	PWM13	–
IO46	GPIO4	I2C1_SDA	RF2_SPI_MI	–	UART2_RX	MC1_3	–	PWM14	–
IO47	GPIO5	SPI_CLK	UART2_RTS	–	I2S_MCLK	–	–	PWM15	–
IO48	GPIO6	SPI_CSN	UART2_CTS	–	I2S_BCLK	–	–	PWM0	–
IO49	GPIO7	SPI_MO	UART2_TX	–	I2S_LRCK	–	–	PWM1	–
IO50	GPIO8	SPI_MI	UART2_RX	–	I2S_DATA_IN	–	–	PWM2	–
IO51	GPIO9	I2C1_SCL	UART1_TX	–	I2S_DATA_OUT	–	–	PWM3	–
IO52	GPIO10	RF1_CTRL0	SPI_CLK	–	–	–	–	PWM4	–
IO53	GPIO11	RF1_CTRL1	SPI_CSN	–	–	–	–	PWM5	–
IO54	GPIO12	RF1_CTRL2	SPI_MO	–	–	–	–	PWM6	–
IO55	GPIO13	RF2_CTRL0	SPI_MI	–	–	I2C1_SCL	–	PWM7	–
IO56	GPIO0	RF2_CTRL1	UART1_TX	–	–	I2C1_SDA	–	PWM8	–
IO57	GPIO1	RF2_CTRL2	UART1_RX	–	–	UART2_TX	–	PWM9	–
IO58	GPIO2	–	RF1_CTRL0	–	SPI_CLK	UART1_TX	–	PWM10	–
IO59	GPIO3	–	RF1_CTRL1	–	SPI_CSN	UART1_RX	–	PWM11	–
IO60	GPIO4	–	RF1_CTRL2	–	SPI_MO	UART2_TX	–	PWM12	–

Pin Name	Mode 0[14]	Mode 1	Mode 2	Mode 3[15]	Mode 4	Mode 5[15]	Mode 6[15]	Mode 7	Note[15]
IO61	GPIO5	–	RF2_CTRL0	–	SPI_MI	UART2_RX	–	PWM13	–
IO62	GPIO6	–	RF2_CTRL1	–	I2C1_SCL	UART2_CTS	–	PWM14	–
IO63	GPIO7	–	RF2_CTRL2	–	I2C1_SDA	UART2_RTS	–	PWM15	–
IO64	GPIO8	–	RF1_SPI_CLK	–	MC0_0	SPI_CLK	–	PWM0	–
IO65	GPIO9	–	RF1_SPI_CSN	–	MC0_1	SPI_CSN	–	PWM1	–
IO66	GPIO10	–	RF1_SPI_MO	–	MC0_2	SPI_MO	–	PWM2	–
IO67	GPIO11	–	RF1_SPI_MI	–	MC0_3	SPI_MI	–	PWM3	–
IO68	GPIO12	–	RF2_SPI_MO	–	MC1_0	UART1_TX	–	PWM4	–
IO69	GPIO13	–	RF2_SPI_MI	–	MC1_1	UART1_RX	–	PWM5	–
IO70	GPIO0	–	RF2_SPI_CLK	–	MC1_2	I2C1_SCL	–	PWM6	–
IO71	GPIO1	–	RF2_SPI_CSN	–	MC1_3	I2C1_SDA	–	PWM7	–
IO72	GPIO2	I2C1_SDA	UART1_RX	–	UART2_RX	RF2_CTRL2	–	PWM8	–

Table 2–17 Internal Level Pinmux

Name	Type[18]	Primary Function	Secondary Function
I2S_DATA_IN	I	I²S	GPIO
I2S_DATA_OUT	O	I²S	GPIO
I2S_BCLK	I/O	I²S	GPIO
I2S_MCLK	I/O	I²S	GPIO
I2S_LRCK	I/O	I²S	GPIO
I2C1_SCL	O	I²C 1	GPIO
I2C1_SDA	I/O	I²C 1	GPIO
I2C2_SCL	O	I²C 2	GPIO
I2C2_SDA[3:0][19]	I/O	I²C 2	GPIO
SPI_CLK	O	SPI	GPIO
SPI_CSN	O	SPI	GPIO
SPI_MO	O	SPI	GPIO
SPI_MI	I	SPI	GPIO
UART1_TX	O	UART 1	GPIO
UART1_RX	I	UART 1	GPIO
UART2_TX	O	UART 2	GPIO
UART2_RX	I	UART 2	GPIO
UART2_CTS	I	UART 2	GPIO
UART2_RTS	O	UART 2	GPIO
TDI	I	JTAG	GPIO
TDO	O	JTAG	GPIO
TCK	I	JTAG	GPIO
TMS	I	JTAG	GPIO
TRSTN	I	JTAG	GPIO
LCD[27:0]	I/O	LCD	GPIO

2.3.2 Register Summary

Table 2–18 lists the pinmux registers and corresponding device memory locations (offset) and descriptions. For each PADIO[*n*] the respective function select bits are ***PIN_MUX[n x 3 + 2:n x 3]***. Each PIN_MUX of PADIO takes 3 bits. Every ten PIN_MUXs form a 4-byte address, bit 31 and bit 30 of the 4-byte address are reserved.

Table 2–18 Register of Upper Level Pinmux

Address	Description
0x9000_002C	PIN_MUX[*n* x 3 + 2:*n x* 3] is function select for PADIO[*n*]. PIN_MUX[31:30] are reserved; *n*: 0 to 9.
0x9000_0030	PIN_MUX[*n* x 3 + 2:*n x* 3] is function select for PADIO[*n* + *10*]. PIN_MUX[31:30] are reserved; *n*: 0 to 9.
0x9000_0034	PIN_MUX[*n* x 3 + 2:*n x* 3] is function select for PADIO[*n* + *20*]. PIN_MUX[31:30] are reserved; *n*: 0 to 9.
0x9000_0038	PIN_MUX[*n* x 3 + 2:*n x* 3] is function select for PADIO[*n* + *30*]. PIN_MUX[31:30] are reserved; *n*: 0 to 9.
0x9000_003C	PIN_MUX[*n* x 3 + 2:*n x* 3] is function select for PADIO[*n* + *40*]. PIN_MUX[31:30] are reserved; *n*: 0 to 9.
0x9000_0040	PIN_MUX[*n* x 3 + 2:*n x* 3] is function select for PADIO[*n* + *50*]. PIN_MUX[31:30] are reserved; *n*: 0 to 9.
0x9000_0044	PIN_MUX[*n* x 3 + 2:*n x* 3] is function select for PADIO[*n* + *60*]. PIN_MUX[31:30] are reserved; *n*: 0 to 9.
0x9000_0048	PIN_MUX[*n* x 3 + 2:*n x* 3] is function select for PADIO[*n* + *70*]. PIN_MUX[31:30] are reserved; *n*: 0 to 9.
0x9000_004C	Pull-up/down the PADIO[31:0]
0x9000_0050	Pull-up/down the PADIO[63:32]
0x9000_0054	Pull-up/down PADIO[72:64]
0x92B0_0000	GPIO data output

[18] The types listed below represent pin type of the primary function. The pin type of the secondary function, GPIO, is I/O.
[19] In I²C mode, any of these four pins may be set as SDA and be switched; whereas, in GPIO mode, the SDA is fixed once being set.

Address	Description
0x92B0_0004	GPIO data input
0x92B0_0008	GPIO output enable
0x92B0_000C	GPIO bypass mode
0x92B0_0010	Set GPIO_O data bit
0x92B0_0014	Clear GPIO_O data bit
0x92B0_0018	GPIO pull enable
0x92B0_001C	GPIO pull high or pull low when pulled is enable
0x92B0_0020	GPIO interrupt enable
0x92B0_0024	GPIO interrupt raw status
0x92B0_0028	GPIO interrupt status after masking
0x92B0_002C	GPIO interrupt mask
0x92B0_0030	GPIO interrupt clear
0x92B0_0034	GPIO interrupt trigger mode.
0x92B0_0038	GPIO interrupt edge trigger by single or both edge
0x92B0_003C	GPIO interrupt trigger level
0x92B0_0040	GPIO pre-scale clock enable
0x92B0_0044	GPIO pre-scale, used to adjust different PCLK frequencies.(1~ffffff)

Table 2–19 Register of Internal Level Pinmux

Address	Description
0x9110_0004	I²S I/O mode (GPIO/normal)
0x9110_00BC	I²S I/O direction/input/output
0x9200_0000	SPI I/O input/output/direction/mode
0x9210_0000	UART 1 I/O mode register (GPIO/normal)
0x9210_0014	UART 1 I/O direction/output/input
0x9220_0000	UART 2 I/O mode register (GPIO/normal)
0x9220_0014	UART 2 I/O direction/output/input
0x9240_001C	I²C 1 I/O input/output/direction/mode
0x9250_001C	I²C 2 I/O input/output/direction/mode
0x92B0_0000	JTAG IO/SEN_GPIO[1:0] output
0x92B0_0004	JTAG IO/SEN_GPIO[1:0] input
0x92B0_0008	JTAG IO/SEN_GPIO[1:0] direction
0x92B0_000C	JTAG IO/SEN_GPIO[1:0] bypass mode
0x92B0_0010	JTAG IO/SEN_GPIO[1:0] set output bit
0x92B0_0014	JTAG IO/SEN_GPIO[1:0] clear output bit
0x92B0_0018	JTAG IO/SEN_GPIO[1:0] pull enable
0x92B0_001C	JTAG IO/SEN_GPIO[1:0] pull high or low
0x92B0_0020	JTAG IO/SEN_GPIO[1:0] interrupt enable
0x92B0_0024	JTAG IO/SEN_GPIO[1:0] interrupt raw status
0x92B0_0028	JTAG IO/SEN_GPIO[1:0] interrupt raw status after mask
0x92B0_002C	JTAG IO/SEN_GPIO[1:0] interrupt mask
0x92B0_0030	JTAG IO/SEN_GPIO[1:0] interrupt clear
0x92B0_0034	JTAG IO/SEN_GPIO[1:0] interrupt trigger mode
0x92B0_0038	JTAG IO/SEN_GPIO[1:0] interrupt edge select
0x92B0_003C	JTAG IO/SEN_GPIO[1:0] interrupt level
0x92B0_0040	JTAG IO/SEN_GPIO[1:0] interrupt de-bounce enable
0x92B0_0044	JTAG IO/SEN_GPIO[1:0] interrupt pre-scale
0x9800_0000	LCD I/O mode register (GPIO/normal)
0x9800_0018	LCD I/O output
0x9800_001C	LCD I/O direction
0x9800_0020	LCD I/O input

2.4 Physical Memory Map

Each hardware function is mapped to a specific memory address. To control the function, assign a value into the corresponding address. For example, setting SPI_GPIO_MODE (0x9200_0000, bit 15) as 0 for SPI1 to act as a normal SPI; otherwise, set 1, for the SPI to act as an internal pinmux GPIO.

Table 2–20 to Table 2–22 show the memory map address ranges of the device. Figure 2–4 shows the memory mapping of each section. For more detailed information, please refer to each function chapter.

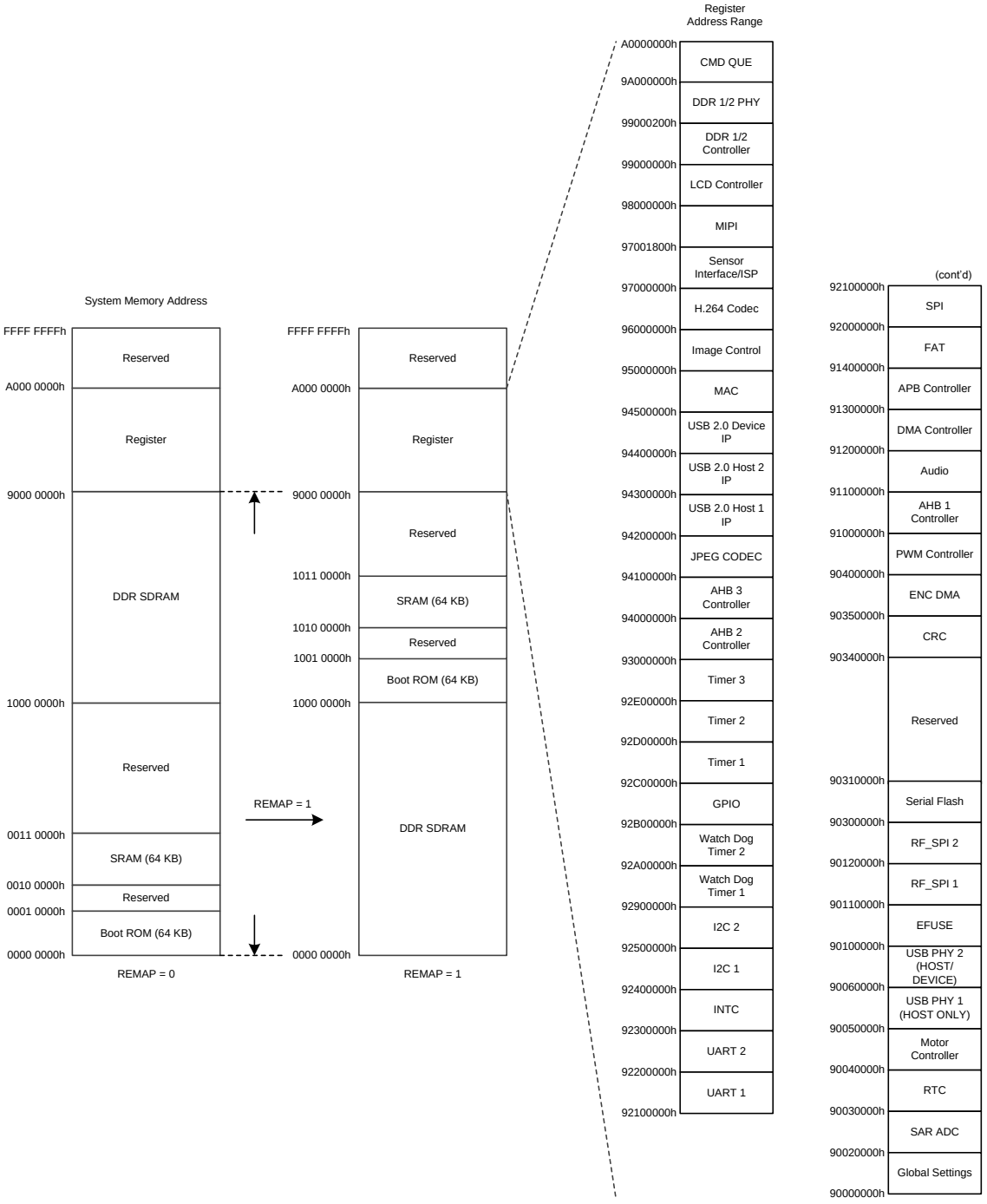


Figure 2–4 Memory Map

Table 2–20 System Memory Address (REMAP = 0)

Region	Address		
	Start	End	Size
Reserved	0xA000_0000	0xFFFF_FFFF	–
Register	0x9000_0000	0x9FFF_FFFF	256 MB
DDR SDRAM	0x1000_0000	0x8FFF_FFFF	2 GB
Reserved	0x0011_0000	0x0FFF_FFFF	–
SRAM	0x0010_0000	0x0010_FFFF	64 KB
Reserved	0x0001_0000	0x000F_FFFF	–
Boot ROM	0x0000_0000	0x0000_FFFF	64 KB

Table 2–21 System Memory Address (REMAP = 1)

Region	Address		
	Start	End	Size
Reserved	0xA000_0000	0xFFFF_FFFF	–
Register	0x9000_0000	0x9FFF_FFFF	256 MB
Reserved	0x1011_0000	0x8FFF_FFFF	–
Boot ROM	0x1000_0000	0x1000_FFFF	64 KB
DDR SDRAM	0x0000_0000	0x0FFF_FFFF	256 MB

Table 2–22 Register Address Ranges

Start Address	End Address	Description
0x9A00_0000	0x9FFF_FFFF	CMD que
0x9900_0200	0x99FF_FFFF	DDR 1/2 PHY
0x9900_0000	0x9900_01FF	DDR 1/2 controller
0x9800_0000	0x98FF_FFFF	LCD controller
0x9700_1800	0x97FF_FFFF	MIPI
0x9700_0000	0x9700_17FF	Sensor interface/ISP
0x9600_0000	0x96FF_FFFF	H.264 codec
0x9500_0000	0x95FF_FFFF	Image controller
0x9450_0000	0x94FF_FFFF	MAC
0x9440_0000	0x944F_FFFF	USB 2.0 device IP
0x9430_0000	0x943F_FFFF	USB 2.0 host 2 IP
0x9420_0000	0x942F_FFFF	USB 2.0 host 1 IP
0x9410_0000	0x941F_FFFF	JPEG codec
0x9400_0000	0x940F_FFFF	AHB3 controller
0x9300_0000	0x93FF_FFFF	AHB2 controller
0x92F0_0000	0x92FF_FFFF	Reserved
0x92E0_0000	0x92EF_FFFF	Timer 3
0x92D0_0000	0x92DF_FFFF	Timer 2
0x92C0_0000	0x92CF_FFFF	Timer 1
0x92B0_0000	0x92BF_FFFF	GPIO
0x92A0_0000	0x92AF_FFFF	Watchdog timer 2
0x9290_0000	0x929F_FFFF	Watchdog timer 1
0x9260_0000	0x928F_FFFF	Reserved
0x9250_0000	0x925F_FFFF	I2C 2
0x9240_0000	0x924F_FFFF	I2C 1
0x9230_0000	0x923F_FFFF	INTC
0x9220_0000	0x922F_FFFF	UART 2
0x9210_0000	0x921F_FFFF	UART 1
0x9200_0000	0x920F_FFFF	SPI
0x9150_0000	0x91FF_FFFF	Reserved
0x9140_0000	0x914F_FFFF	FAT
0x9130_0000	0x913F_FFFF	APB controller
0x9120_0000	0x912F_FFFF	DMA controller
0x9110_0000	0x911F_FFFF	Audio
0x9100_0000	0x910F_FFFF	AHB 1 controller

Start Address	End Address	Description
0x9041_0000	0x90FF_FFFF	Reserved
0x9040_0000	0x9040_FFFF	PWM controller
0x9036_0000	0x903F_FFFF	Reserved
0x9035_0000	0x9035_FFFF	ENC DMA
0x9034_0000	0x9034_FFFF	CRC
0x9030_0000	0x9030_FFFF	Serial flash
0x9013_0000	0x902F_FFFF	Reserved
0x9012_0000	0x9012_FFFF	RF_SPI 2
0x9011_0000	0x9011_FFFF	RF_SPI 1
0x9010_0000	0x9010_FFFF	EFUSE
0x9007_0000	0x900F_FFFF	Reserved
0x9006_0000	0x9006_FFFF	USB PHY 2 (host/device)
0x9005_0000	0x9005_FFFF	USB PHY 1 (host only)
0x9004_0000	0x9004_FFFF	Motor controller
0x9003_0000	0x9003_FFFF	RTC
0x9002_0000	0x9002_FFFF	SAR ADC
0x9000_0000	0x9000_0FFF	Global settings

2.5 Device Support

SONiX offers an extensive line of tools available for the SN93700 Series including the software development kit (SDK) and RTOS based development environments (See Appendix A) to support the development of device based applications.
For a complete listing of development-support tools for the SN93700 Series multimedia network platforms, visit the SONiX web site on the worldwide web at http://www.sonix.com.tw. For information on pricing and availability, please contact the nearest SONiX sales office or an authorized distributor.

3 System

3.1 ARM Subsystem
3.2 System Controller (Global Settings)
3.3 Clock Configuration
3.4 Operating Frequencies
3.5 Interrupt Controller (INTC)
3.6 CRC-*N*
3.7 Direct Memory Access Controller (DMAC)
3.8 DDR2/DDR SDRAM Memory Controller (DDR12C)
3.9 Power Management
3.10 Boot Mode
3.11 Device Reset

3.1 ARM Subsystem

The SN93700 Series is comprised of an ARM subsystem that contains all of the necessary components required to provide the ARM926EJ-S master control of the overall device system which includes the components of the ARM subsystem, peripherals, and external memories.

The ARM subsystem manages system functions such as system-level initialization, configuration, application interface, application command execution, connectivity functions, interface and control of the subsystem. With a large program memory space and fast switching capability, the ARM subsystem can master and perform the function. This helps the SN93700 Series be suitable for complex, multi-tasking and general-purpose control tasks.

The ARM subsystem consists of the following components:

- ARM926EJ-S RISC processor, including:
  – Coprocessor 15 (CP15)
  – MMU
  – 16 KB I-cache
  – 16 KB D-cache
  – ARM® Jazelle® technology
- System control peripherals
  – ARM Interrupt Controller
  – PLL Controller

The ARM subsystem manages/controls all the device peripherals.

- Advanced High-performance Bus (AHB)
  The SN93700 Series uses the AHB port of the ARM926EJ-S to connect the ARM subsystem to the configuration bus and the external memories. Arbiters are employed to arbitrate access to the separate D-AHB and I-AHB by the configuration bus and the external memories bus.

- Advanced Peripheral Bus (APB)
  The APB bridge responds to transaction requests from the currently enabled bus master. The AHB transactions are converted into APB transactions.

- Advanced eXtensible Interface (AXI)
  The AXI protocol supports for unaligned data transfer using byte strobes. All AXI buses are 64-bit data width for the SN93700 Series.

3.1.1 ARM926EJ-S CPU

The SN93700 Series integrates an ARM926EJ-S as the main control CPU. The ARM926EJ-S performs multi-tasking applications with its 4GB address space, memory management, high performance, small die size, and low power features while supporting the 32-bit ARM.

The ARM926EJ-S processor supports the ARM subsystem debug architecture and includes the logic for hardware and software debug. The ARM926EJ-S also provides a complete high performance subsystem.

For complete details on the ARM9, please refer to the ARM926EJ-S technical reference manual available at http://www.arm.com

3.1.2 Memory Management Unit (MMU)

The ARM926EJ-S MMU provides virtual memory features required by Linux. A set of two level page tables that is stored in the main memory to control the address translation, permission checks, and memory region attributes for both data and instruction accesses. The MMU uses a single unified translation look-aside buffer (TLB) to cache the information held in the page tables. Features of MMU include:

- Standard ARM architecture version 4 and version 5 MMU mapping sizes, domains and access protection scheme.
- Mapping sizes:
  – 1 MB (sections)
  – 64 KB (large pages)
  – 4 KB (small pages)
  – 1 KB (tiny pages)
- Access permissions for large pages and small pages that can be specified separately for each quarter of the page
- Hardware page table walks
- Invalidate entire TLB, using CP15 register 8.
- Invalidate TLB entry, selected by MVA, using CP15 register 8.
- Lockdown of TLB entries, using CP15 register 10.

3.1.3 Caches

The size of the I-cache and D-cache each is 16 KB. Features of the caches include:

- Virtual index, virtual tag, and addressed using the modified virtual address (MVA)
- Four-way set associative, with a cache line length of eight words per line (32 bytes per line) and with two dirty bits in the D-cache.
- D-cache supports write-through and write-back (or copy back) cache operation, selected by memory region using the C and B bits in the MMU translation tables.
- Critical-word first cache refilling.
- Cache lockdown registers enable control over the cache ways that are used for allocation on a line fill providing a mechanism for both lockdown and controlling cache corruption.
- D-cache stores the physical address tag (PA TAG) corresponding to each D-cache entry in the TAG RAM to be used during the cache line write-backs in addition to the Virtual Address TAG stored in the TAG RAM. With the MMU not involved in D-cache write-back operations, the possibility of TLB missing related to the write-back address can be avoided.
- Cache maintenance operations provide efficient invalidation of the entire D-cache or I-cache, regions of the D-cache or I-cache, and regions of virtual memory

The write buffer is used for all writes to a non-cacheable and bufferable region, write-through region and write misses to a write-back region. A separate buffer is incorporated in the D-cache for holding write-back for cache line evictions or cleaning of dirty cache lines. The main write buffer has 16-word data buffer and a four-address buffer. The D-cache write-back has eight data word entries and a single address entry.

3.1.4 CP15

The ARM926EJ-S system control coprocessor (CP15) is used to configure and control I-caches and D-caches, MMU, and the other ARM subsystem functions. The CP15 registers are programmed using the MRC and MCR instructions when the ARM subsystem is in a privileged mode such as supervisor or system mode.

3.2 System Controller (Global Settings)

The system controller enables the device to provide a customized solution by enabling/disabling each IP. It is easy to find a balance between high performance and low power consumption through different settings.

Features of the system controller include:

- Power down mode and wakeup selection
- Change settings of the PLL and clock rate control for operation in different clock frequencies
- Disable the peripheral clocks by the clock gating registers
- Select pinmux functions and setting pull-up/down

3.2.1 Register Summary

Table 3–1 Registers of Global Settings

Address range: 0x9000_0000 to 0x9000_0FFF

Offset	Description
0x00000	Power-down control Test mode
0x00004–0x00008	Chip clock rates MAC PHY clock on/off
0x0000C	CPU PLL selector DDR DQS
0x00010	Power down domain control
0x00014	Memory mode selector Demux on/off AHB control
0x00018	Bus arbiter control
0x0001C–0x00020	Clock gatings
0x00024–0x00028	Reserved
0x0002C–0x00054	Pinmux controls
0x00058–0x000A0	Reserved
0x000A4	ASIC chip ID
0x000A8	Supply DDR V_{REF} on/off JTAG I/O control I2C selector DDR PHY on/off LVD control Misc. function controls
0x000AC	Built-in 100, 300 and 800 MHz PLLs control
0x000B0–0x000B4	Built-in LCD PLL control
0x000B8	Trimming value source selector
0x000BC–0x00FFF	Reserved

3.3 Clock Configuration

3.3.1 Oscillators

The device requires one primary reference clock source to provide the major clock input. The reference clock frequency may be generated either by crystal input or by external oscillator. The reference clock input is provided by the XIN pin.

Table 3–2 Oscillators Electrical Requirements and Characteristics

Parameter	MIN.	TYP.	MAX.	UNIT
Start-up time (from power up until oscillating at stable frequency)	–	–	4	ms
Crystal oscillation frequency	–	12	–	MHz
Crystal oscillation mode	Fundamental only			–
Crystal frequency stability	30			ppm

3.3.2 Phase-Locked Loops (PLL)

The device requires one primary reference clock. The reference 12 MHz clock frequency may be generated either by crystal input or the external oscillator. The reference clock drives five separate phase-locked loop (PLL) controllers (PLL800, PLL480, PLL300, PLL100, and LCDPLL) through XIN and XOUT.

PLL800 generates the clocks required by the ARM926EJ-S and the rest of the peripherals. PLL480 generates the clock required by the USB host and device interfaces. PLL300 generates the clock required by the H.264 codec and LCD controller. PLL100 generates the clock required by the EtherMAC and TV-out. LCDPLL generates the clock required by the LCD outputting to panel. These frequencies are detailed in Table 3–3.

Table 3–3 PLL Clock Frequency

Clock	Required Frequency	Description
PLL800	564 MHz to 804 MHz	Main system clocks
PLL480	480 MHz	USB host and device
PLL300	264 MHz to 336 MHz	H.264
PLL100	100 MHz	EtherMAC and TV-out
LCDPLL	Up to 150 MHz	LCD controller

Table 3–4 PLL List

PLL	Used by	Output Frequency
PLL800OUT	CPU	402 MHz max.
	DDR	402 MHz max.
	AHB 0	For ROM, SRAM, and CPU located on AHB 0 optional using either PLL480, but not using PLL300/PLL100/LCDPLL 201 MHz max.
	AHB 3	For MAC, JPEG, USB host and USB device located on AHB 3, but not using PLL480/PLL300/PLL100/ LCDPLL 268 MHz max.
	AXI 0	For image controller located on AXI 0, but not using PLL480/ PLL300/PLL100/LCDPLL 268 MHz max.
	AXI 2	For ISP located on AXI 2, but not using PLL480/ PLL300/PLL100/LCDPLL 268 MHz max.
PLL480OUT	AHB 1	For audio, DMAC, SF, CRC-N, and FAT located on AHB 1, but not using PLL800/PLL300/PLL100/ LCDPLL 120 MHz max.
	AHB 2	Reserved
	APB	For timer, GPIO, I²C, PWM, SPI, UART, MC, ADC, e-fuse, and audio ADC/DAC located on APB, but not using PLL800/ PLL300/PLL100/LCDPLL 48 MHz max.
	Timer	Max 48 MHz
	USB device	480 MHz
	USB host	480 MHz
	UART	12 MHz max.
PLL300OUT	H.264	324 MHz max.
	AXI 1	For H.264 codec located on AXI 1, but not using PLL800/ PLL480/PLL100/LCDPLL 324 MHz max.
	AXI 3	For LCD controller located on AXI 3, but not using PLL800/PLL480/PLL100/LCDPLL 324 MHz max.
PLL100OUT	EtherMAC, RMII PHY	100 MHz

PLL	Used by	Output Frequency
	TV-out	25 MHz
	Timers	10 MHz
	UART	10 MHz
LCDPLLOUT	LCD	LCD output, up to 150 MHz

3.4 Operating Frequencies

The reference clock for the five independently controlled PLLs on the device is a single crystal input. PLL800 generates the frequencies needed for the ARM and the rest of the peripherals. The USB 2.0 PHY has an embedded PLL480. Table 3–4 shows the maximum speed for each of the major blocks.

Features of the PLL are:

- Provide primary system clock
- Programmable PLL divider value
- Programmable PLL multiplier value
- Accept clock input or internal oscillator input

Table 3–5 Maximum Operating Frequencies of CPU, DDR, and Bus

Function	Maximum Frequency
ARM926EJ-S	402 MHz
DDR2 SDRAM	402 MHz
AMBA AXI bus 0	268 MHz
AMBA AXI bus 1	324 MHz
AMBA AXI bus 2	268 MHz
AMBA AXI bus 3	324 MHz
AMBA AHB bus 0	201 MHz
AMBA AHB bus 1	120 MHz
AMBA AHB bus 2	96 MHz
AMBA APB bus	48 MHz

3.5 Interrupt Controller (INTC)

The interrupt controller (INTC) provides a software interface to the interrupt system. Based on the ARM subsystem, the SN93700 Series has one level of interrupts: Interrupt Request (IRQ) for general interrupts.

The sequence of events for the interrupts is:

1. INTC collects interrupt signals from various modules
2. INTC generates the IRQ interrupt signals to the ARM.

The properties of all interrupt signals can be configured by the INTC registers which are mapped to the APB. The INTC supports up to 53 interrupt sources listed in Table 3–6. The software initializes edge or level sensitivity and checks the source of the interrupt when it receives IRQ events from the ARM. The registers of INTC are at base address 0x9230_0000.

Features of the interrupt controller (INTC) are:

- Up to 64 standard interrupt (IRQ) inputs
- Interrupts can be routed to the IRQ
- Provides edge-triggered /level-triggered interrupt sources with positive and negative directions
- De-bounce circuits for the interrupt input sources
- Enable or disable any interrupt source independently

3.5.1 Interrupt Source Assignment

The SN93700 Series has 53 IRQs. Table 3–6 is a list of interrupt sources (IRQ) with IRQ numbers and device vectors.

Table 3–6 Interrupt Source (IRQ)

IRQ No.	Device Vector	Initial Value[20]
0	TIMER1_INT	0
1	TIMER2_INT	0
2	TIMER3_INT	0
3	USB20_Device INT	0
4	USB20 HOST 2 INT	0
5	USB20 HOST 1 INT	0
6	LCD_INT	0
7	MIPI_INT	0
8	SEN_HSYNC_INT	0
9	ISP_WIN_END_INT	1
10	SYN_VSYNC	0
11	ISP_DIS_INT	0
12	IMG_TX_INT	0
13	H264_ENCODE_INT	0
14	JPEG_INT	0
15	RF1_INT	0
16	RF2_INT	0
17	MAC_INT	–
18	UART1_INT	–
19	UART2_INT	–
20–24	Reserved	–
25	SF_INT	0
26	CRC_OK_INT	–
27	Reserved	–
28	GPIO_INT	0
29	DMA_INT	0
30	ADO_R_INT	0
31	ADO_W_INT	0
32	AHB0_AHBC_INT	–
33	AHBC1_INT	–
34	AHBC2_INT	–
35	AHBC3_INT	–
36	I2C1_INT	–
37	I2C2_INT	–
38–40	Reserved	–
41	SPI_INT	–
42	APB_INT	–
43	DDR_CTRL_INT	–
44	WDOG_INT	–
45	RTC_ALARM	–
46	RTC_WAKEUP	–
47	CMDQUE_INT	–
48	KEY	–
49	RTC_GPIO0	–
50	RTC_GPIO1	–
51	REG_RW_ERR	–
52	ISP_MD_IRQ	–

[20] "–" = Unknown

3.5.2 Register Summary

Table 3–7 Registers of INTC

Address range: 0x9230_0000 to 0x923F_FFFF

Offset	Description
0x00000	Interrupt[31:0] status
0x00004	Interrupt[31:0] source enable
0x00008	Interrupt[31:0] clear
0x0000C	Interrupt[31:0] trigger mode
0x00010	Interrupt[31:0] level
0x00014	Interrupt[31:0] flag
0x00018–0x0004C	Reserved
0x00050	Interrupt controller version
0x00054	Number of supported interrupt inputs
0x00058	Interrupt[52:32]de-bounce status
0x0005C	Reserved
0x00060	Interrupt[52:32] status
0x00064	Interrupt[52:32] source enable
0x00068	Interrupt[52:32] clear
0x0006C	Interrupt[52:32] trigger mode
0x00070	Interrupt[52:32] level
0x00074	Interrupt[52:32] flag
0x00078	Interrupt[52:32] de-bounce status
0x0007C–0xFFFFC	Reserved

3.6 CRC-*N*

The cyclic redundancy check (CRC) module is used to get a CRC code from an arbitrarily *N*-bit data word and a programmable generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. The CRC-*N* calculation unit helps compute a software signature during runtime to be compared with a reference signature generated at link-time and stored at a given memory location to verify the integrity of the flash memory.

The CRC module in the SN93700 Series supports maximum 32 bits with a programmable polynomial. A CRC takes a data stream or a block of data as input and generates an *N*-bit output that can be appended to the data and used as a checksum. The CRC-*N* provides DMA mode to process data, a region of data can be specified in DRAM by setting the start address and size of the data to do a CRC calculation on.

The SN93700 Series CRC-*N* supports the following operations and features:

- Built-in CRC-*N* Mod codec
- Maximum 32 bits with a programmable polynomial. For example, CRC-16-CCITT is

$$x^{16} + x^{12} + x^5 + 1$$

- Programmable hex value (e.g. CRC-16-CCITT is 0 x 1021)
- DMA mode

3.6.1 Register Summary

Table 3–8 Registers of CRC-*N*

Address range: 0x9034_0000 to 0x903F_FFFF

Offset	Description
0x00000	CRC-*N* control
0x00004	CRC-*N* start address for DMA
0x00008	CRC-*N* line size
0x0000C	CRC-*N* line number
0x00010	CRC-*N* line gap
0x00014	CRC-*N* initial, output XOR values and orders
0x00018	CRC-*N* programmable polynomial

Offset	Description
0x0001C	CRC-*N* and check sum result
0x00020–0xFFFFC	Reserved

3.7 Direct Memory Access Controller (DMAC)

The direct memory access (DMA) controller is designed to enhance system performance. System efficiency is improved with high-speed data transfers among the system and devices by reducing processor-interrupt generation. The DMA controller provides up to four configurable channels for memory-to-memory transfers with the shared buffers.

Features of the DMA are:

- Four configurable DMA channels
- Memory-to-memory transfers
- Group round-robin arbitration scheme with 4 priority levels
- Chain transfer
- Transfer with 8/16/32-bit data width
- Hardware handshaking
- Big-endian and little-endian

3.7.1 Register Summary

Table 3–9 Registers of DMA Controller

Address range: 0x9120_0000 to 0x912F_FFFF

Offset	Description
0x00000	Interrupt status
0x00004	Interrupt for terminal count status
0x00008	Interrupt for terminal count clear
0x0000C	Interrupt for error/abort status
0x00010	Interrupt for error/abort clear
0x00014	Terminal count status
0x00018	Error/abort status
0x0001C	Channel enable status
0x00020	Channel busy status
0x00024	Main configuration control
0x00028	Synchronize
0x0002C	Reserved
0x00030	DMAC version
0x00034	DMAC features
0x00038–0x000FC	Reserved
0x00100	Channel 0 control
0x00104	Channel 0 configuration
0x00108	Channel 0 source
0x0010C	Channel 0 destination
0x00110	Channel 0 linked list pointer address
0x00114	Channel 0 transfer size
0x00118–0x0011C	Reserved
0x00120	Channel 1 control
0x00124	Channel 1 configuration
0x00128	Channel 1 source
0x0012C	Channel 1 destination
0x00130	Channel 1 linked list pointer address
0x00134	Channel 1 transfer size
0x00138–0x0013C	Reserved
0x00140	Channel 2 control
0x00144	Channel 2 configuration
0x00148	Channel 2 source
0x0014C	Channel 2 destination
0x00150	Channel 2 linked list pointer address
0x00154	Channel 2 transfer size

Offset	Description
0x00158–0x0015C	Reserved
0x00160	Channel 3 control
0x00164	Channel 3 configuration
0x00168	Channel 3 source
0x0016C	Channel 3 destination
0x00170	Channel 3 linked list pointer address
0x00174	Channel 3 transfer size
0x00178–0xFFFFC	Reserved

3.8 DDR2/DDR SDRAM Memory Controller

The DDR2/DDR memory controller supports access to the DDR2 or DDR SDRAM of industry standard simultaneously and achieves high-bandwidth and low-latency access with both high-performance and low-power applications. The DDR2/DDR SDRAM memory controller can be used for program and data storage.

Features of the DDR2/DDR SDRAM controller are:

- Supports DDR2 or DDR
- SDRAM data rate up to 800 Mbps (DDR2-800 or DDR-500)
- Supports SSTL18 for DDR IO
- Detection of address collision to avoid a data coherency violation at the same address
- Multi-port arbitration between different masters
- Access to the DDR2/DDR mode registers
- DDR2 memory on-die termination
- Flexible paging policy and reordering queue to optimize bandwidth and latency
- Automatic refresh timer to reduce the refresh overhead
- Power-down and self-refresh modes

NOTE SSTL2 is NOT supported for DDR.

The DDR2/DDR memory controller is the main interface to the DDR2/DDR memory. Master peripherals, such as DMAC and the CPU can access the DDR2/DDR memory controller directly. The DDR2/DDR memory controller performs all memory-related background tasks such as opening and closing banks, refreshes, and command arbitration.

3.9 Power Management

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry to avoid the flip-flops having to switch states for power saving. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred. For efficient power management, the SN93700 Series supports clock gating control for audio, CRC, timer, FAT, CMDQUE, MC 0, MC 1, DDR, MIPI, ISP, EtherMAC, SF, SAR ADC, SPI, H.264 codec, UART 1, UART 2, JPEG codec, USB host 1, USB host 2, USB device, PWM, LCD, MIPI, IMC_CTL, RF 1, and RF 2.

3.10 Boot Mode

Figure 3–1 shows the boot flow of the SN93700 Series.

- The test mode is for CP/FT test.
- System state
  - PwrOff: Previous system state is power off.
  - Normal HS (High Speed) Mode: Previous system state is normal run. Boot loader takes over after reset and runs in high speed mode.
  - Normal LP (Low Power) Mode: Previous system state is normal run. Boot loader takes over after reset and runs in low speed mode.

  – BypassBt: Previous system state is normal run. Bypass boot loader after reset.
  – Error: Previous system state is error. Boot loader leads the system into ISP mode.
  – When error is shown as the system state, the serial flash reads error or receives “ESC” key from UART to enter the ISP mode (firmware upgrade mode). The firmware upgrade is possible via USB and UART.
- Default ROM code condition
  – Remap = 0
  – High speed mode

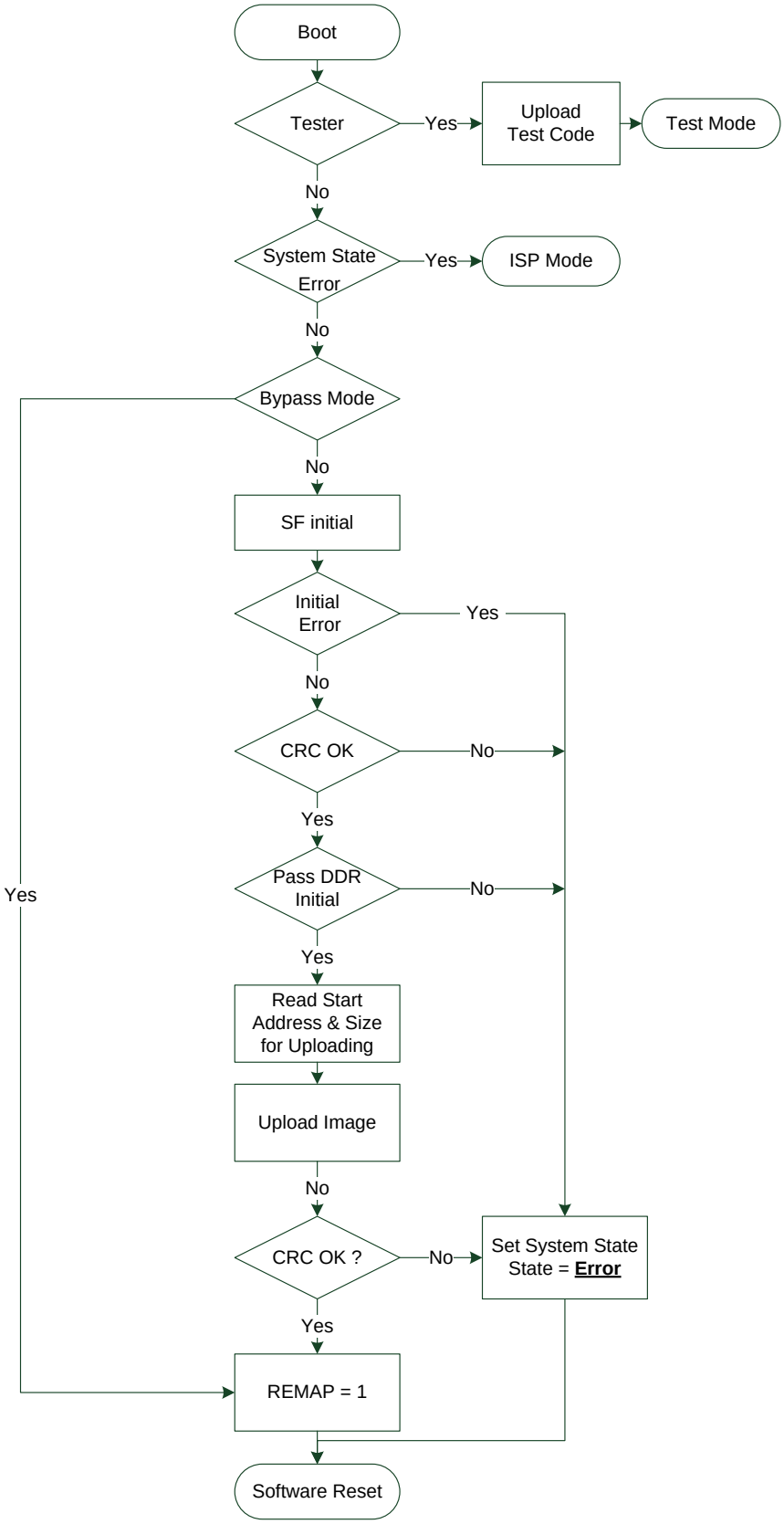


Figure 3–1 Flow Chart of the Boot Mode Procedure

3.11 Device Reset

Table 3–10 Reset Types

Type	Initiator	Effect
Power-On-Reset (POR)	RSTN pin low and power off, can be used on the PCB assembly.	Total reset of the chip (cold reset); DDR memory data are lost. All components on the PCB assembly resets.
Warm Reset	RSTN pin low	Resets everything on the chip to the default values without RTC internal registers[21].
Watchdog Reset	Watchdog timer triggers RSTN pin low	Resets everything on the chip to default values without RTC_CTL and RTC internal registers[21].

[21] RTC internal registers are in the range of 90030000h–90030074h without 90030100h.

4 Multimedia

4.1 Video
4.2 Audio

4.1 Video

For multi-stream video encoding, decoding and image analysis, the SN93700 Series includes parallel and MIPI interfaces[22], image signal processing (ISP) engine, JPEG codec, H.264 codec, image controller and LCD/TV interfaces. This section provides an overview of the SN93700 Series video process.

4.1.1 Image Input Interface

The SN93700 Series supports parallel LVCMOS sensor interface and serial MIPI sensor interface. As shown in Figure 4–1, both interfaces are connected to the ISP input. Only one interface can be operated at a time, although the LVCMOS or MIPI pins are hooked up to different video sources on the PCB assembly.

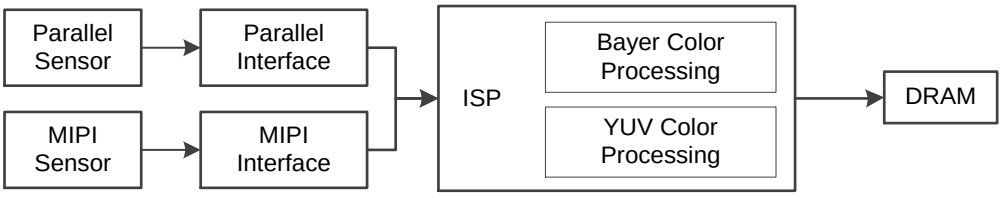


Figure 4–1 Sensor Input Interface

The sensor input interfaces support parallel (1.8V/3.3V LVCMOS, single pixel) and single-lane x4 or dual-lane x2 MIPI signaling. The sensor interfaces support the following sensor formats:

- Image resolution: Super HD (2304 x 1296), QXGA (2048 x 1536), UXGA (1600 x 1200), 1080P (1920 x 1080), SXGA (1280 x 1024), 720P (1280 x 720), and VGA (640 x 480)
- Image data format: 10-bit Bayer RAW (max 90 MP/sec) and 8-bit YUY2 (max 120 MP/sec)
- Output clock: 96 MHz / *n* or 120MHz / *n* MHz output clock to CMOS sensor
- *n* = sensor master clock driver (range: 2 to 255)
- I²C: Industrial standard 2-wire serial interface
- MIPI-CSI2: Four sets of one data LAN per clock LAN or two sets of two data LANs per clock LAN (bitrate: up to 1 Gbps)

I. Image Input Modes

There are two sensor input interfaces supported, one single-pixel LVCMOS and one MIPI serial input.

- Single-pixel LVCMOS: Up to 10-bit parallel sensor interface.
- Pixel clock: SEN_PCLK
- Sensor clock: SEN_CLK
- Pixel data[9:0]: SEN_D[9:0]
- HSYNC: SEN_HSYNC
- VSYNC: SEN_VSYNC

[22] Unavailable for SN93701 and SN93711.

MIPI serial input: single-lane x4 or dual-lane x2 MIPI-CSI2 serial sensor interface.

- MIPI clock lane: MIPI1_DPCK0, MIPI1_DNCK0, MIPI1_DPCK1, MIPI1_DNCK1, MIPI2_DPCK0, MIPI2_DNCK0, MIPI2_DPCK1, and MIPI2_DNCK1
- MIPI data lane: MIPI1_DP0, MIPI1_DN0, MIPI1_DP1, MIPI1_DN1, MIPI2_DP0, MIPI2_DN0, MIPI2_DP1, and MIPI2_DN1

II. Timing

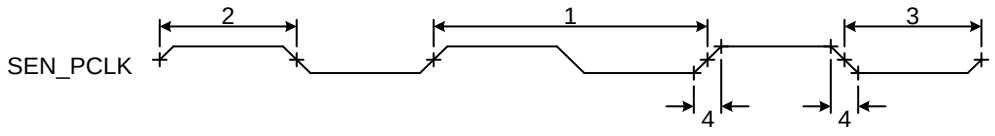


Figure 4–2 Sensor Interface SEN_PCLK Timing

Table 4–1 Timing Requirements for SEN_PCLK in Parallel Slave Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{c(S_PCK)}$	Cycle time, SEN_PCLK	8.33	–	ns
2	$t_{w(SEN_PCLKH)}$	Pulse duration, SEN_PCLK high	3.80	–	ns
3	$t_{w(SEN_PCLKL)}$	Pulse duration, SEN_PCLK low	3.80	–	ns
4	$t_{t(SEN_PCLK)}$	Transition time, SEN_PCLK	–	2.00	ns

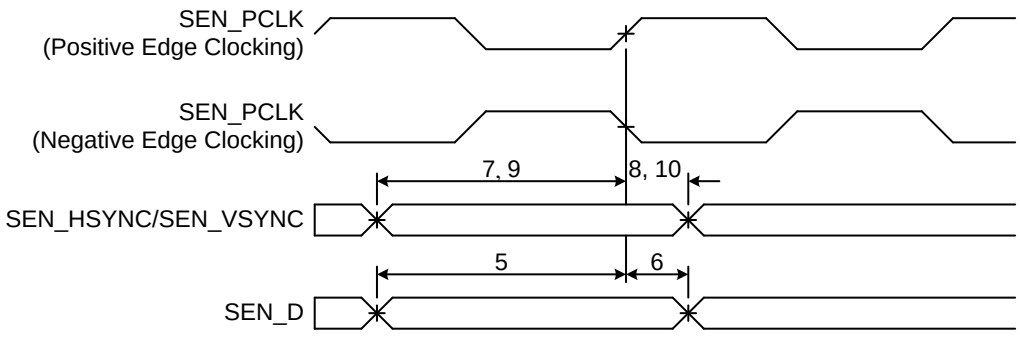


Figure 4–3 Sensor Interface Slave Mode Input Data Timing

Table 4–2 Timing Requirements for Input Data in Parallel Slave Mode

No.	Parameter			Device		Unit
				MIN.	MAX.	
5	$t_{su(S_IMG-SEN_PCLK)}$	Setup time, SEN_D valid before SEN_PCLK edge	Positive Edge Negative Edge	3	–	ns
6	$t_{h(SEN_PCLK-S_IMG)}$	Hold time, SEN_D valid after SEN_PCLK edge	Positive Edge Negative Edge	2	–	ns
7	$t_{su(S_HSYNC-SEN_PCLK)}$	Setup time, SEN_HSYNC valid before SEN_PCLK edge	Positive Edge Negative Edge	3	–	ns
8	$t_{h(SEN_PCLK-S_HSYNC)}$	Hold time, SEN_HSYNC valid after SEN_PCLK edge	Positive Edge Negative Edge	2	–	ns
9	$t_{su(S_VSYNC-SEN_PCLK)}$	Setup time, SEN_VSYNC valid before SEN_PCLK edge	Positive Edge Negative Edge	3	–	ns
10	$t_{h(SEN_PCLK-S_VSYNC)}$	Hold time, SEN_VSYNC valid	Positive Edge	2	–	ns

No.	Parameter			Device		Unit
				MIN.	MAX.	
		after SEN_PCLK edge	Negative Edge			

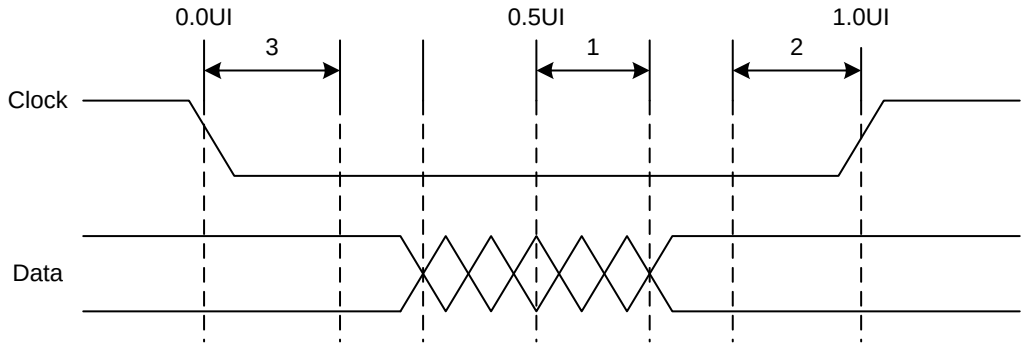


Figure 4–4 Input Data Timing in MIPI Master/Slave Mode

Table 4–3 Timing Requirements for MIPI Master/Slave Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	t_{SKEW}	Data to clock skew measured at the transmitter	-0.15	0.15	UI
2	$t_{su(DATV-CLK)}$	Data to clock setup time at receiver	0.2	–	UI
3	$t_{h(CLK-DATV)}$	Clock to data hold time at receiver	0.2	–	UI
4	UI_{INST}	One data bit time (instantaneous)	1	12.5	ns
5	$t_{c(CLK)}$	Period of dual data rate clock	2	25	ns
6	Clock freq.	Maximum clock rate defined in MIPI spec.	–	500	MHz
7	Data freq.	Data rate in single data lane condition	–	1000	MHz

4.1.2 Image Signal Processing (ISP)

The image data from the sensor input interface is in either Bayer RAW pattern or YCbCr format. The data in Bayer pattern is processed by Bayer color processing module first including lens shading correct (LSC), wide dynamic range (WDR), defect pixel correction (DPC), and 2D/3D NR. The data in YCbCr format is processed by the YUV color processing module.

Features of the ISP include:

- Color processing
- AE histogram statistics
- AWB window statistics
- AF edge window statistics
- Auto/manual defect-pixel concealment
- Lens shading compensation for R/G/B channel
- Color interpolation (less false color)
- Individual digital color gain control for R/Gr/Gb/B channels
- Individual digital color gain control for Y/Cb/Cr channels
- Pixel offset (optical black) compensation for R/Gr/Gb/B channels
- Configurable 2D/3D noise reduction
- Alpha-blending on-screen display (OSD)
- Purple fringe suppression

- Advanced anti-aliasing filter
- Configurable advanced edge enhancement
- Programmable gamma table for Y channel
- Programmable gamma table for RGB correction
- Programmable color conversion matrix for R/G/B input
- Programmable hue and saturation
- Configurable windowing function after processed image
- Motion detection report ver.2
- Two lines x 32 characters text overlap with 8 x 16, 12 x 16, and 16 x 16 pixels for each character (x 1, x 2, x 3, x 4, x 5, x 6, x 7, and x 8 scale support) and 24-bit true color (YUV888)
- Flip and mirror
- Software watermark
- Image black blocking (private mask) with 16 x 12 ROI of full image
- Highlight/backlight compensation enhance
- Video resizer: clamping/scaler/frame rate drop
- Configurable vertical lens distortion correction
- Digital image stabilization
- Video source scaling down
- For Super HD (2304 x 1296), QXGA (2048 x 1536), UXGA (1600 x 1200), 1080P (1920 x 1080), SXGA (1280 x 1024), 720P (1280 x 720), VGA (640 x 480) sensors, combined scaling and windowing function provides similar view angle for SXGA (1280 x 1024)/720P (1280 x 720)/SVGA (800 x 600)/VGA (640 x 480)/CIF (352 x 288)/QVGA (320 x 240)/QCIF (176 x 144)/QQVGA (160 x 120) output resolution.
- The scaling and frame rate adjusting engine are separately controlled for three video streams
- Features for 1st and 2nd video streams are OSD, flip and mirror, and LPF and scaling
- The 3rd video stream supports an optional Y only, RGB, YUV420 or YUV422 formats

The ISP block diagram is as shown in Figure 4–5. First ISP sequentially processes the image data received in either Bayer or YCbCr format from the image sensor. ISP includes vLDC, LSC, WDR, DPC, and DN. RGB color processing AE, AWB, gamma correction, domain transfer and color suppress are then applied. The scaling and filter processing module supports horizontal and vertical down-scaling, YUV color filter, and edge enhancement. The processed data are then passed to the DRAM via three different video channels.

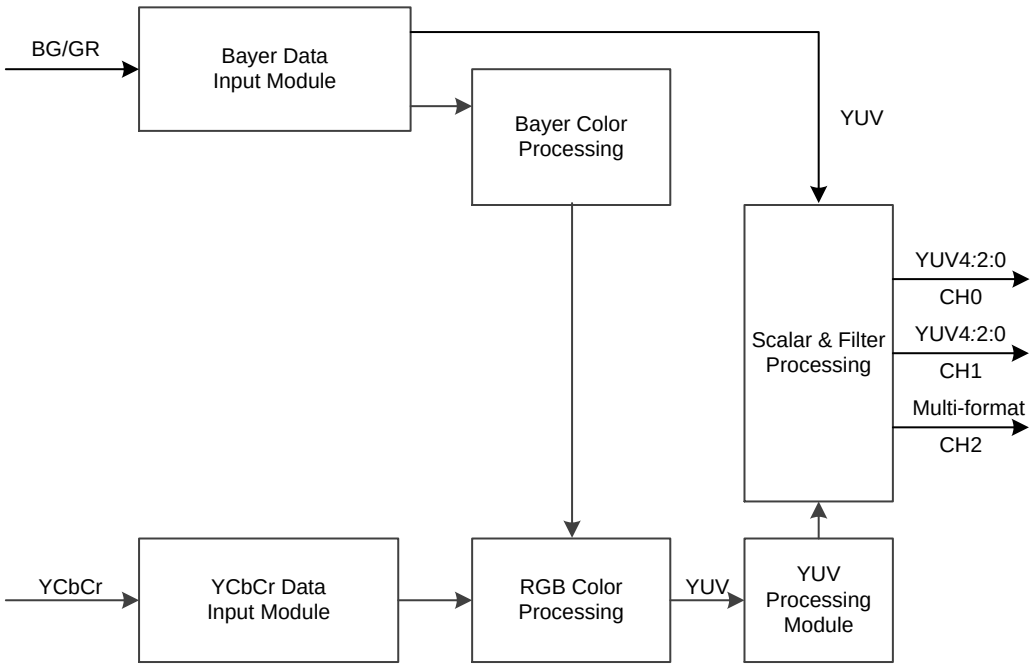


Figure 4–5 Image Process Flow

4.1.3 Video Codecs

The SN93700 Series video engine is a high-performance, low power, and multi-stream multimedia information device. As shown in Figure 4–6, there are two parts of the video processing module, one image controller and one JPEG codec.

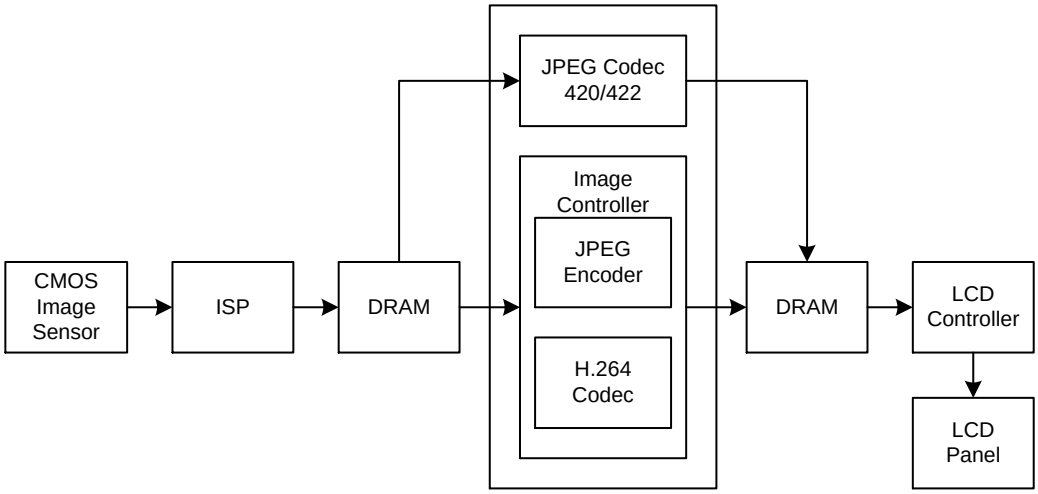


Figure 4–6 Video Codec Block Diagram

I. Image Controller

The image controller includes one H.264 encoder and decoder, one JPEG encoder, one pixel-based data stamp overlay engine, and one video down-scaler. The H.264 video codec is a hardware-based H.264 video codec engine. The JPEG encoder generates a single JPEG snapshot. Applications may aggregate multiple JPEG images into one MJPEG video stream. This image controller supports time-sharing for several YUV420 video inputs. The encoder fetches YUV420 video raw data from DRAM and outputs H.264 bit-stream and JPEG bit-stream simultaneously. When the scaling down feature is unused, the video engine generates one H.264 stream and one JPEG video stream. As shown in Figure 4–7, when the scaling down feature is used once, one H.264 stream in original resolution, one scaled down H.264 stream, one JPEG stream, one scaled down JPEG steam, and one scaled down YUV420 video in raw format are being generated with time sharing.

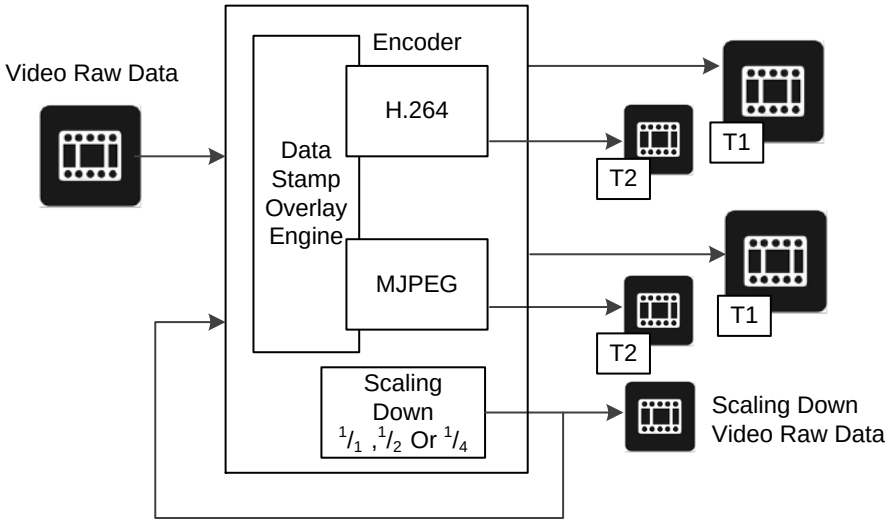


Figure 4–7 Video Encoders of the Image Controller

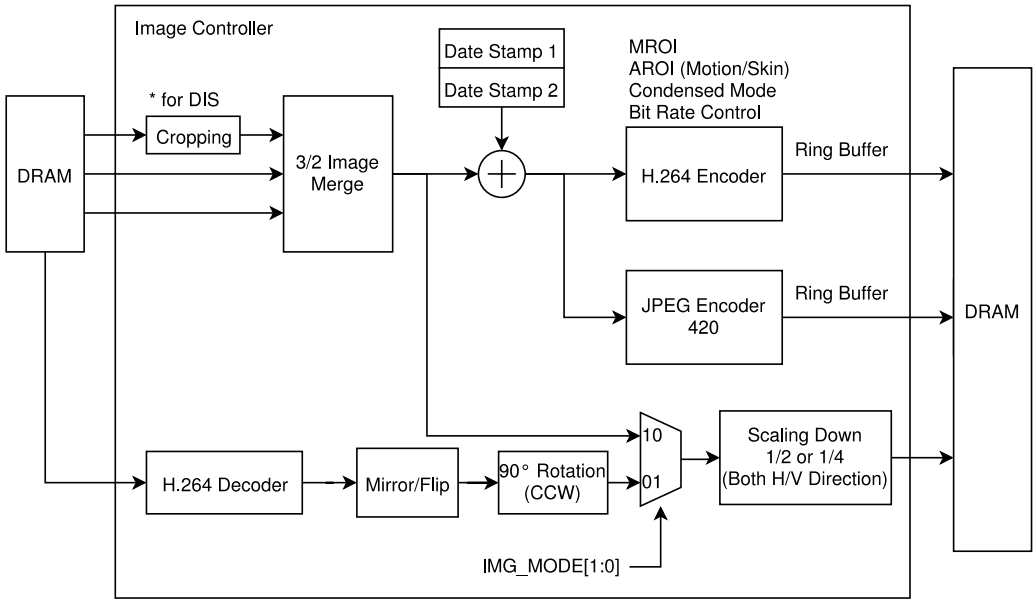


Figure 4–8 Image Controller Block Diagram

As shown in Figure 4–8, the image controller includes six parts:

- H.264 encoder
  – Input format: 8-bit MB-based YUV4:2:0
  – Input resolution: QCIF (176 x 144) to 1080P (1920 x 1088)
  – Output format: encoded elementary stream compatible with ISO/IEC14496-10 high profile @Level4.1:
  – Features
    ▪ I & P picture types
    ▪ CAVLC/CABAC entropy
    ▪ All 4 x 4 (nine modes) and 16 x 16 (four modes) intra prediction modes
    ▪ All 16 x 16, 16 x 8, 8 x 16, 8 x 8, 8 x 4, 4 x 8, and 4 x 4 inter prediction modes

- ▪ Adjustable QP for Y and C to provide programmable compression ratio
- ▪ 4 x 4 integer DCT
- ▪ In-loop de-blocking filter (with on/off function)
- ▪ Motion estimation search range: V: -16 to 16 pixels; H: -13 to 32 pixels
- ▪ Quarter-pel motion vector precision
- ▪ Multi-slice coding (one slice is limited to a multiple of MB lines)

– Rate Control:
- ▪ Frame Level: Constant Quantization Mode, Constant Bitrate Mode, Limited Bitrate Mode.
- ▪ Macro-block rate control (MbRc): Bitrate stability enhancement, human visual quality enhancement, MROI and AROI detection, condense mode

• H.264 decoder
– Input format: Encoded elementary stream compatible with ISO/IEC14496-10 high profile @Level4.1
– Input resolution: QCIF (176 x 144) to 1080P (1920 x 1088)
– Output format: 8-bit MB-based YUV4:2:0
– Features
- ▪ I & P picture types
- ▪ CAVLC/CABAC entropy
- ▪ All 4 x 4 (nine modes) and 16 x 16 (four modes) intra prediction modes
- ▪ All 16 x 16, 16 x 8, 8 x 16, 8 x 8, 8 x 4, 4 x 8, and 4 x 4 inter prediction modes
- ▪ Motion estimation search range: V: -16 to 16 pixels; H: -33 to 32 pixels

– Supports image rotation, flip, and mirror functions; each function can be enabled separately

• JPEG encoder
– Input format: 8-bit MB-based YUV4:2:0
– Maximum resolution: 3MP (2048 x 1536, 4:3; 2304 x 1296, 16:9)
– Output format: JPEG, YUV420 bit-stream, 8 bits data
– Features
- ▪ Baseline discrete cosine transform (DCT)
- ▪ Fixed Huffman table (two AC, two DC, typical Huffman table at ISO-IEC 10918-1)
- ▪ 128 bytes quantization tables for Y and C provide programmable compression ratio

• Image merging
– Merging two or three source inputs of the same resolution to one image
– Maximum horizontal resolution: 1920 pixels

• Video down-scaler
– Scaling down resolution
– Scaling ratio including 1/1, 1/2, and 1/4 for H and V directions simultaneously

• Pixel-based data stamp overlay engine
– Supports data stamp overlay before H.264/JPEG encoder
– Maximum 256 user defined colors
– 8-level transparency weighting option
– Scaling up character (x 1, x 2, and x 4 for both X and Y coordinates)
– Two sets of date stamp that share the same pallet table

II. JPEG Codec

In addition to the built-in JPEG encoder of the image controller, there is a JPEG codec for dedicated image JPEG compression and decompression. Functional blocks of the JPEG codec are shown as below.

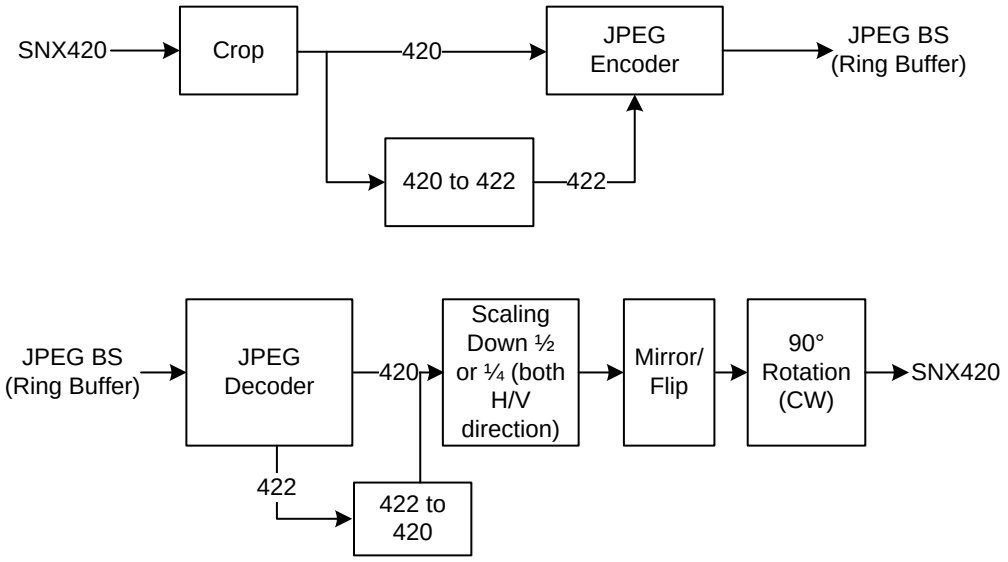


Figure 4–9 JPEG Codec Block Diagram

Features of the JPEG codec include:

- Baseline DCT, fixed Huffman table (two AC, two DC, typical Huffman table at ISO/IEC 10918-1)
- JPEG File Interchange Format (JFIF)
- Format: YCbCr422 and 420
- Scalable resolution from QQVGA (160 x 120) to 12M in 16:9 and 4:3 (4096 x 3072 and 4608 x 2592). The unit of a step is X (16 pixels for YCbCr422 and 420), Y (8 lines for YCbCr422; 16 lines for YCbCr420).
- Sharing DCT, zig-zag, quantizer and FIFO for encoder and decoder
- Operate at JPEG-encoder or JPEG-decoder mode
- Requires three single-port SRAM (DCT 128 x 12, ZigZag 128 x 11, Quantizer 128 x 8)
- 1920 x 1080 @30 fps encoder/decoder when the clock is operating at 185 MHz under the condition that F/W overhead is less than 5 ms per frame.
- Encoder data input format: The data in the DRAM is 8 bits in SONiX 420 format only (8-bit YCbCr data input and standard JPEG 420/422 data sequence inside of the encoder).
- Encoder data output format: JPEG bit-stream, 8-bit data output.
- Decoder data input format: JPEG bit-stream, 8-bit data input.
- Decoder data output format: The data in the DRAM is in 8-bit SONiX 420 format only (8-bit YCbCr data output and standard JPEG 420/422 data sequence inside of the decoder).
- Standard JPEG 420/422 data sequence
  - 8 x 8 pixel sequence in one block: From left to right, from up to down.
  - Block sequence in one macro block:
    - 422 is Y0, Y1, Cb, Cr, Y2, Y3, Cb, Cr
    - 420 is Y0, Y1, Y2, Y3, Cb, Cr
  - Macro block sequence in one frame: From left to right, from up to down.
- Ring buffer for JPEG bitstream output.
- Cropping function at the encoder input only. Starting position of the cropped video can move at two pixels per step in the horizontal direction and two lines per step in the vertical direction.
- H size: 9-bit (unit: 16 pixels)
- V size: 9-bit (unit: 8 lines)
- Image rotation, flip/mirror function (0°, 90°, 180°, 270°) at decoder output.
- 1/1, 1/2 or 1/4 down-scaling at the decoder output (both horizontal and vertical direction).
- Maximum horizontal resolution of 8064.
- Maximum vertical resolution of 4032.

4.1.4 Image Output Interface (LCD/TV)

The LCD controller supports most popular digital LCD panels and CVBS (TV-out) interfaces. It transfers LCD image data from an internal display buffer and outputs to external pins for the LCD panel.
The output resolution is from 160 x 120 to 1920 x 1080 with a 256-color graphic OSD layer. The LCD controller has four channel inputs with cropping and scaling functions to provide various arrangements of position and size on the LCD panel.

Features of the LCD controller include:

- LCD interface
  - GPIO mode
  - AU UPS051 8-bit data width
  - AU UPS051 6-bit data width
  - AT3210 LCD controller mode
  - ST7528 LCD controller mode
  - IST3101 LCD controller mode
  - RGB dummy
  - DE mode 24-bit data width
  - AU LCD controller mode
  - 8080 8-bit data width, 2 bytes for 1 pixel, RGB565
  - 8080 8-bit data width, 3 bytes for 1 pixel, RGB888
  - 8080 9-bit data width, 2 bytes for 1 pixel, RGB666
  - 8080 16-bit data width, RGB565
  - YUV422 sensor interface
  - BT.656/BT.601
  - CVBS output
- 4-channel inputs with cropping function, SONiX YUV420 format
- Two sets of fine scaling up/down (range: 4 x 4 to 1/4 x 1/4) with 9-taps FIR LPF and cropping output
- Two sets of rough 2 x 2 scaling up
- One dedicated TE pin for tear-effect avoidance sync input
- Color dithering for RGB565 and RGB666 LCD panel
- Graphical OSD supporting FHD (1920 x 1080) resolution
- OSD with a color palette that supports 255 colors and a transparent color for each pixel.
- Clock source: Fractional-N PLL, max up to 150 MHz for FHD 60 fps
- Built-in JPEG decoder supporting JPEG YUV422 bitstream with resolution up to 720P (1280 x 720)
- PiP (Picture-in-Picture)

Block diagram of the LCD controller is shown in Figure 4–10. The image data comes from the image buffer of DRAM. After being cropped by each LCD channel, a display channel is assigned to one of the two fine scaling sets (FS0 or FS1) that are classified depending on the scaling ratio. Colors and quality of the image can be corrected by Y gamma and UV gain. After merging with OSD, the image data is converted to the designated signals of LCD format to output to an external LCD/TV panel.

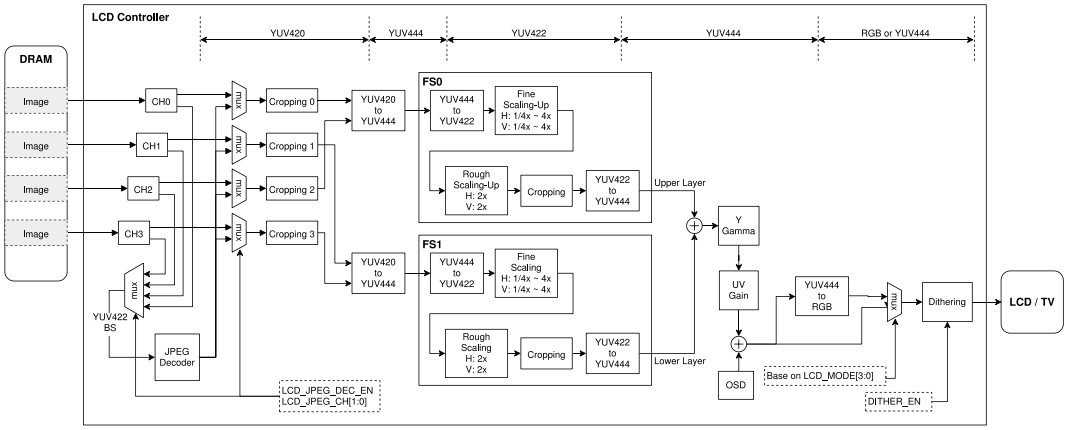


Figure 4–10 LCD Controller Block Diagram

The SN93700 Series provides three display layers of laminated construction on panel. As shown in Figure 4–11, the upper layer image data is overlaid on the lower layer.

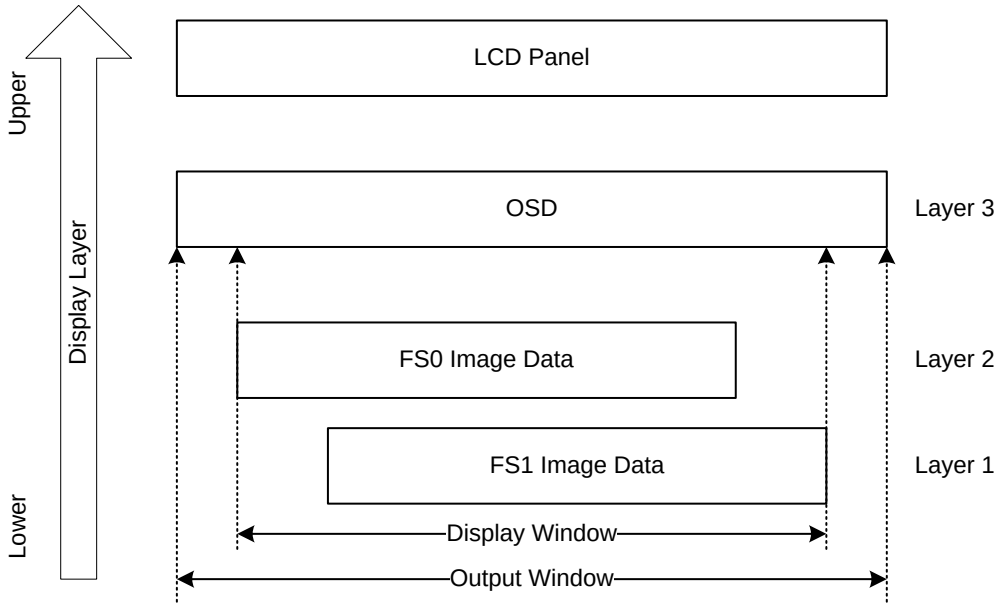


Figure 4–11 LCD Layers

I. Register Summary

Table 4–4 Registers of LCD Controller

Address ranges: 0x9800_0000 to 0x98FF_FFFF

Offset	Description
0x00000	LCD main function
0x00004	TV mode and setting
0x00008	TV setting1
0x0000C	TV setting2
0x00010	LCD read/write command
0x00014	LCD read/write data
0x00018	LCD GPIO output

Offset	Description
0x0001C	LCD GPIO output enable
0x00020	LCD GPIO input
0x00024	LCD start address for channel 0
0x00028	LCD start pixel and line of cropping image for channel 0
0x0002C	LCD cropping image size for channel 0
0x00030	Reserved
0x00034	LCD start address for channel 1
0x00038	LCD start pixel and line of cropping image for channel 1
0x0003C	LCD cropping image size for channel 1
0x00040	Reserved
0x00044	LCD start address for channel 2
0x00048	LCD start pixel and line of cropping image for channel 2
0x0004C	LCD cropping image size for channel 2
0x00050	Reserved
0x00054	LCD start address for channel 3
0x00058	LCD start pixel and line of cropping image for channel 3
0x0005C	LCD cropping image size for channel 3
0x00060	Reserved
0x00064	LCD fine scaling 0 enable and LPF coefficient
0x00068	LCD fine scaling 0 LPF coefficient 1
0x0006C	LCD fine scaling 0 horizontal and vertical scaling factor
0x00070	LCD fine scaling 0 start pixel and line of cropping output image
0x00074	LCD fine scaling 0 size of cropping output image
0x00078	LCD fine scaling 1 enable and LPF coefficient
0x0007C	LCD fine scaling 1 LPF coefficient 1
0x00080	LCD fine scaling 1 horizontal and vertical scaling factor
0x00084	LCD fine scaling 1 start pixel and line of cropping output image
0x00088	LCD fine scaling 1 size of cropping output image
0x0008C–0x00120	Reserved
0x00124	LCD active pixel size for LCD output
0x00128	LCD dummy pixel and line before active region
0x0012C	LCD dummy pixel and line after active region
0x00130	LCD pixel clock speed , RGB sequence and dither function
0x00134	LCD output pulse width setting
0x00138	LCD Y gamma 0
0x0013C	LCD Y gamma 1
0x00140	LCD Y gamma 2
0x00144	LCD Y gamma 3
0x00148	LCD Y gamma 4
0x0014C	LCD UV gain
0x00150	LCD OSD main
0x00154	LCD OSD line size
0x00158	Reserved
0x0015C	LCD palette table read for OSD
0x00160	LCD palette table address
0x00164	LCD palette data write
0x00168	LCD BT.601/BT.656 mode
0x0016C	BT.601/BT.656 field 1 VSYNC start line
0x00170	BT.601/BT.656 field 1 VSYNC end line
0x00174	BT.601/BT.656 field 2 VSYNC start line
0x00178	BT.601/BT.656 field 2 VSYNC end line
0x0017C	BT.601/BT.656 field 1 identification change line
0x00180	BT.601/BT.656 field 2 identification change line
0x00184	LCD start position of window 0
0x00188	LCD start position of window 1
0x0018C	LCD start position of window 2
0x00190	LCD start position of window 3
0x00194–0x001C0	Reserved
0x001C4	Start address of OSD data in DRAM
0x001C8	LCD OSD X direction region
0x001CC	LCD OSD Y direction region
0x001D0	TV test image Y/Cb/Cr input

Offset	Description
0x001D4	LCD default background color while no pixel output
0x001D8	JPEG decoder function in LCD
0x001DC	JPEG decoder status in LCD
0x001E0	JPEG decoder Q-table control
0x001E4	JPEG decoder trigger to read Q-table
0x001E8	JPEG decoder Q-table data
0x001EC–0x001F8	Reserved
0x001FC	LCD controller version
0x00200–0xFFFFC	Reserved

II. Timing

The SN93700 Series LCD controller has two types of timing, CPU mode and non-CPU mode. Features of the LCD controller in CPU mode include:

- AT3210 LCD controller mode
- ST7528 LCD controller mode
- IST3101 LCD controller mode
- 8080 8-bit data width, 2 bytes for 1 pixel, RGB565
- 8080 8-bit data width, 3 bytes for 1 pixel, RGB888
- 8080 9-bit data width, 2 bytes for 1 pixel, RGB666[23]
- 8080 16-bit data width, RGB565[23]

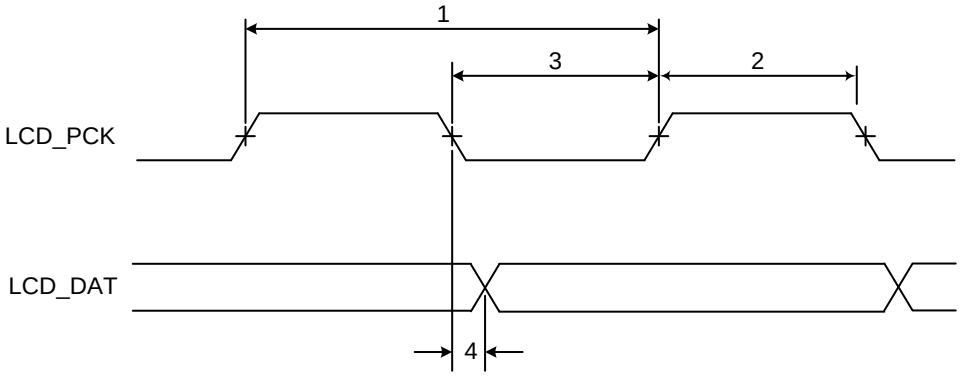


Figure 4–12 LCD Controller Timing in CPU Mode

Table 4–5 Switching Characteristics for LCD Controller in CPU Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{c(LCD_PCK)}$	Cycle time, LCD_PCK	6.73	–	ns
2	$t_{w(LCD_PCKH)}$	Pulse width, LCD_PCKH	0.35 ($t_{c(LCD_PCK)}$)	–	ns
3	$t_{w(LCD_PCKL)}$	Pulse width, LCD_PCKL	0.35 ($t_{c(LCD_PCK)}$)	–	ns
4	$t_{d(LCD_PCK-LCD_DAT)}$	Delay time, LCD_PCK falling to LCD_DAT	-1	1.5	ns

[23] Unavailable for SN937x0, x = a variable number

Features of the LCD controller in non-CPU mode include:

- AU UPS051 8-bit data width
- AU UPS051 6-bit data width
- RGB dummy
- DE mode 24-bit data width
- AU LCD controller mode
- YUV422 sensor interface
- BT.656/BT.601

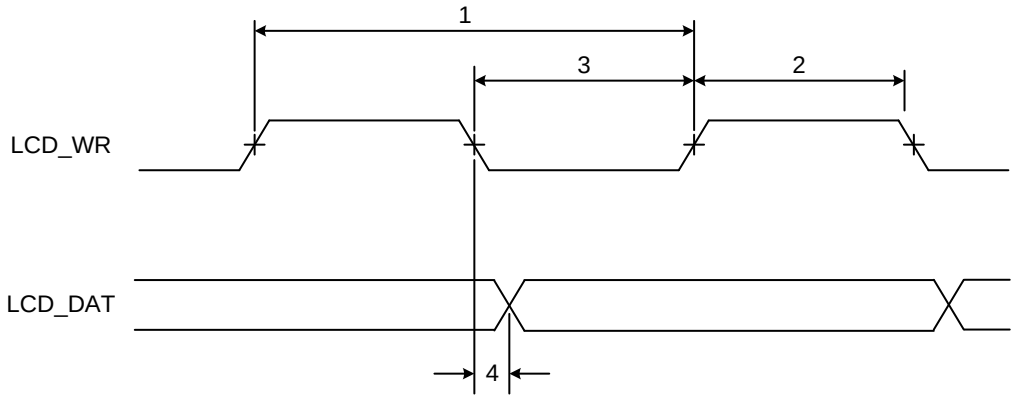


Figure 4–13 LCD Controller Timing in Non-CPU Mode

Table 4–6 Switching Characteristics for LCD Controller in Non-CPU Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{c(LCD_WR)}$	Cycle time, LCD_WR	13.46	–	ns
2	$t_{w(LCD_WRH)}$	Pulse width, LCD_WRH	0.35 ($t_{c(LCD_WR)}$)	–	ns
3	$t_{w(LCD_WRL)}$	Pulse width, LCD_WRL	0.35 ($t_{c(LCD_WR)}$)	–	ns
4	$t_{d(LCD_WR-LCD_DAT)}$	Delay time, LCD_WR falling to LCD_DAT	-1	1.5	ns

4.2 Audio

The audio function includes an I²S controller, DRAM buffer controller, digital adjustment functions, MS-ADPCM/A-law codec, sigma-delta ADC, and R2R DAC. In addition, the play and record function from external ADC/DAC components are provided in the I²S interface. Figure 4–14 is a functional block diagram that shows the relationship between the audio controller and peripherals.

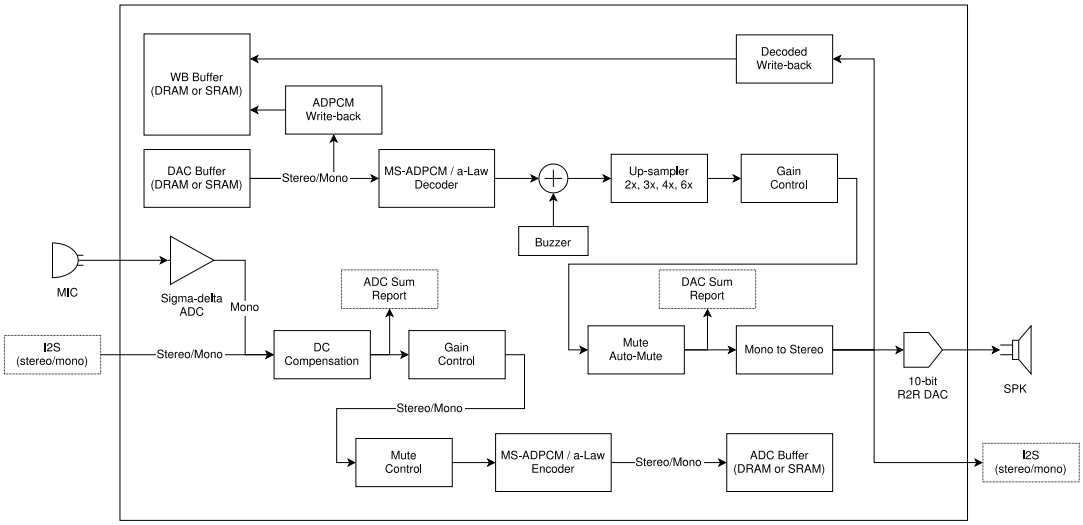


Figure 4–14 Audio Block Diagram

Features of the audio include:

- Internal mono 16-bit sigma-delta boost gain
- Internal mono 10-bit R2R DAC
- I²S full-duplex synchronous serial interface
- DMA ring buffer controller to or from DRAM
- 8K/11.025K/16K/24K/32K/44.1K/48K sampling rate
- Signed/unsigned data format
- 8/16-bit resolution
- Built-in hardware audio MS-ADPCM codec
- Built-in hardware audio A-law codec
- Sample summary report
- DC compensation
- Buffer control for data
- Gain control
- Mute function
- Auto-mute function

4.2.1 I²S Interface

The I²S audio interface includes I2S_LRCK, I2S_BCLK, I2S_DATA_IN and I2S_DATA_OUT. Simultaneous recording and playback at the same sampling rate are implemented with these four pins. Simultaneous recording and playback at different sampling rates is not supported. I²S interface is configured as master or slave mode. In the master mode, the I2S_LRCK and I2S_BCLK are outputs to external devices. In the slave mode, the I2S_LRCK and I2S_BCLK are inputs from external devices. I2S_ DATA_IN is an input of the serial recording data, and I2S_ DATA_OUT is an output of the serial playback data.

Other than the pins described above, there is an additional pin, I2S_MCLK. It is used as a master clock for better synchronization between systems. In the master mode, I2S_LRCK and I2S_BCLK are generated by either an external or internally generated master clock. If the external master clock is selected, I2S_MCLK is an input and becomes the master clock source. If the internally generated master clock is selected, I2S_MCLK is an output and outputs the internally generated master clock. In the slave mode, although I2S_LRCK and I2S_BCLK are driven by an external device, I2S_MCLK is also configured as an output and outputs the internally generated master clock to the external device such that a crystal component can be omitted.

Features of the I²S audio interface include:

- Master or slave modes
- 8/16-bit resolution
- 8K/11.025K/16K/24K/32K/44.1K/48K sampling rate
- Full-duplex communication at the same sampling rate
- Signed or unsigned data format

I. Internal Pinmux

The I²S pins have two pinmux levels. The internal pinmux option of I2S_DATA_IN, I2S_DATA_OUT, I2S_BCLK, I2S_MCLK and I2S_LRCK is GPIO (pin type: I/O). For upper level pinmux options, see Table 2–16..

II. Timing

The I²S is a standard interface for general use. Since the audio controller supports mono (left channel) only, the data is valid in first 8/16-bit from MSB in left channel of its timing diagram.

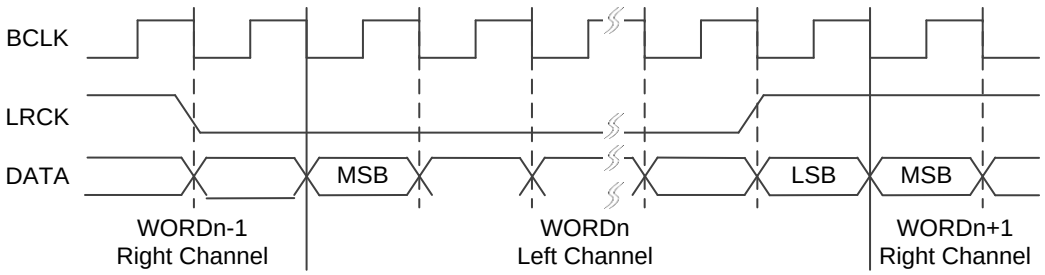


Figure 4–15 I²S Timing

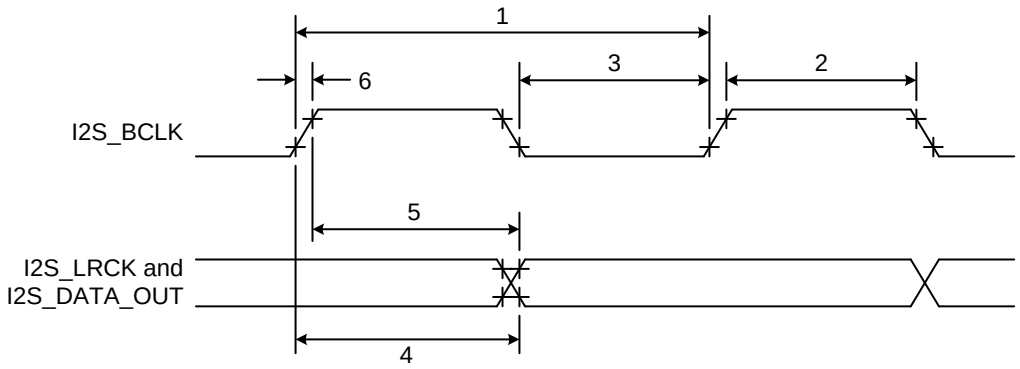


Figure 4–16 I²S Transmitter Timing

Table 4–7 Switching Characteristics for I²S Master Transmitter

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{c(BCK)}$	Cycle time, I2S_BCLK	200[24]	10200	ns
2	$t_{w(BCKH)}$	Pulse width, I2S_BCLK high	0.4 ($t_{c(BCK)}$)	–	ns
3	$t_{w(BCKL)}$	Pulse width, I2S_BCLK low	0.4 ($t_{c(BCK)}$)	–	ns
4	$t_{d(BCK-LRCK_SDX)}$	Delay time, I2S_BCLK rising edge to I2S_DATA_OUT output	–	0.5 ($t_{c(BCK)}$) + 5	ns
5	$t_{h(BCK-LRCK_SDX)}$	Output hold time, I2S_DATA_OUT valid after receive rising edge of I2S_BCLK	0.5 ($t_{c(BCK)}$) - 5	–	ns
6	$t_{r(BCK)}$	Rise time, I2S_BCLK	–	20	ns

Table 4–8 Input Timing Requirements for for I²S Slave Transmitter

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{c(BCK)}$	Cycle time, I2S_BCLK	80	10200	ns
2	$t_{w(BCKH)}$	Pulse width, I2S_BCLK high	0.35 ($t_{c(BCK)}$)	–	ns
3	$t_{w(BCKL)}$	Pulse width, I2S_BCLK low	0.35 ($t_{c(BCK)}$)	–	ns
6	$t_{r(BCK)}$	Rise time, I2S_BCLK	–	0.15 ($t_{c(BCK)}$)	ns

Table 4–9 Switching Characteristics for I²S Slave Transmitter

No.	Parameter		Device		Unit
			MIN.	MAX.	
4	$t_{d(BCK-LRCK_SDX)}$	Delay time, I2S_BCLK rising edge to I2S_DATA_OUT output	–	0.5 ($t_{c(BCK)}$) + 15	ns
5	$t_{h(BCK-LRCK_SDX)}$	Output hold time, I2S_DATA_OUT valid after receive rising edge of I2S_BCLK	0.35 ($t_{c(BCK)}$)	–	ns

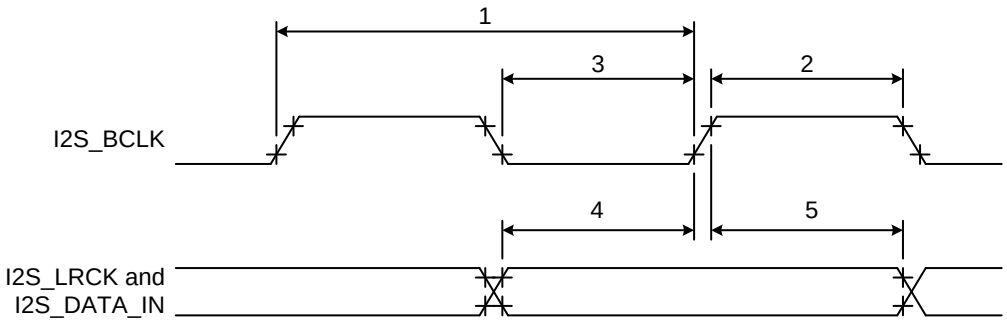


Figure 4–17 I²S Receiver Timing

[24] The minimum period of the master clock is 40 ns and the minimum period of BCK is two master clock cycles. But considering the period of BCK is three master clock cycles, the minimum pulse width (high or low) of BCK is 0.33 ($t_{c(BCK)}$) which violates the I²S input timing requirement. To meet the input timing requirement, the minimum period of BCK is five master clock cycles.

Table 4–10 Switching Characteristics for I²S Master Receiver

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{c(BCK)}$	Cycle time, I2S_BCLK	200[24]	10200	ns
2	$t_{w(BCKH)}$	Pulse width, I2S_BCLK high	0.4 ($t_{c(BCK)}$)	–	ns
3	$t_{w(BCKL)}$	Pulse width, I2S_BCLK low	0.4 ($t_{c(BCK)}$)	–	ns

Table 4–11 Input Timing Requirements for for I²S Master Receiver

No.	Parameter		Device		Unit
			MIN.	MAX.	
4	$t_{su(SDR-BCK)}$	Setup time, I2S_DATA_IN valid before I2S_BCLK rising edge	0.2 ($t_{c(BCK)}$)	–	ns
5	$t_{h(BCK-SDR)}$	Output hold time, I2S_DATA_OUT valid after receive rising edge of I2S_BCLK	2	–	ns

Table 4–12 Input Timing Requirements for I²S Slave Receiver

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{c(BCK)}$	Cycle time, I2S_BCLK	80	10200	ns
2	$t_{w(BCKH)}$	Pulse width, I2S_BCLK high	0.35 ($t_{c(BCK)}$)	–	ns
3	$t_{w(BCKL)}$	Pulse width, I2S_BCLK low	0.35 ($t_{c(BCK)}$)	–	ns
4	$t_{su(SDR-BCK)}$	Setup time, I2S_DATA_IN valid before receive rising edge of I2S_BCLK	0.2 ($t_{c(BCK)}$)	–	ns
5	$t_{h(BCK-SDR)}$	Output hold time, I2S_DATA_OUT valid after receive rising edge of I2S_BCLK	2	–	ns

4.2.2 Audio Codec

The audio codec includes MS-ADPCM, G.711 a-law, and G.711 μ-law. Both contain encoder and decoder for I²S, ADC, and the DAC data paths.

I. R2R DAC

R2R DAC converts the digital audio data from the audio controller to analog signal and output it to external pins. Features of the R2R DAC include:

- 10-bit mono unsigned digital input
- 8K/11.025K/16K/24K/32K/44.1K/48K sampling rate
- 4-bit PGA gain control
- THD + N (0 dB): -51.8 dB
- SNR: 57 dB (at 48 kHz sampling rate)
- Dynamic range: 57 dB

II. Sigma-delta ADC

Sigma-delta ADC transforms the analog audio signal from external pins to the digital audio data converter and transfers the data to the audio controller. Features of the Sigma-delta ADC include:

- Mono sound input
- MIC (single-ended/differential/single-ended and differential) input depending on the package
- 16-bit digital data
- 8K/11.025K/16K/24K/32K/44.1K/48K sampling rate

- PGA gain control
- MIC boost
- THD + N (0 dB): -76.8 dB
- SNR: 93 dB (at 48 kHz sampling rate)
- Dynamic range: 93 dB

4.2.3 Register Summary

Table 4–13 Registers of Audio Codec

Address ranges: 0x9110_0000 to 0x911F_FFFF

Offset	Description
0x00000	Audio controller version
0x00004	ADC and DAC main function
0x00008	Reserved
0x0000C	Audio a-law codec
0x00010	Audio ADPCM codec
0x00014	ADPCM Codec frame size
0x00018	Interrupt status
0x0001C	Interrupt clear
0x00020	Audio recording buffer start address
0x00024–0x0003C	Reserved
0x00040	Decreasing size for audio recording buffer data count
0x00044–0x0005C	Reserved
0x00060	Audio recording buffer data count
0x00064–0x0007C	Reserved
0x00080	Audio recording buffer control
0x00084–0x0008C	Reserved
0x00090	Audio playback buffer start address
0x00094	Decreasing size for audio playback buffer data count
0x00098	Audio playback buffer data count
0x0009C	Audio playback buffer control
0x000A0–0x000AC	Reserved
0x000B0	Audio clock source
0x000B4	Audio clock rate
0x000B8	Reserved
0x000BC	Audio I/O GPIO mode
0x000C0	Audio input gain and mute control
0x000C4	Audio input peak-detection threshold
0x000C8	Audio input peak-detection report
0x000CC	Audio DC compensation
0x000D0	Buzzer control
0x000D4	Buzzer volume level
0x000D8	Buzzer trigger level
0x000DC–0x000E0	Reserved
0x000E4–0x000E8	Buzzer count checking
0x000EC	Buzzer sine wave table
0x000F0	Buzzer level index
0x000F4	Buzzer index trigger
0x000F8–0x000FC	Reserved
0x00100	ADPCM encoded write back buffer control
0x00104	ADPCM encoded write back buffer start address
0x00108	Decreasing size for ADPCM write back buffer data count
0x0010C	ADPCM write back buffer data count
0x00110	ADPCM write back buffer interrupt flag
0x00114	Decoder write back buffer control
0x00118	Decoder write back buffer start address
0x0011C	Decreasing size for decoder write back buffer
0x00120	Decoder write back buffer data count
0x00124	Decoder write back interrupt flag
0x00128	Audio input buffer current index address
0x0012C	Audio output buffer current index address

Offset	Description
0x00130	ADPCM write back buffer current index address
0x00134	Decoder write back buffer current index address
0x00138–0x0013C	Reserved
0x00140	DAC output gain and mute control
0x00144	DAC output data report
0x00148	DAC volume
0x0014C–0x001FC	Reserved
0x00200–0x003FC	Sigma-delta ADC data
0x00400–0xFFFFC	Reserved

5 Peripheral and Operating Specifications

5.1 General Purpose Input/Output (GPIO)
5.2 Inter-integrated Circuit (I²C)
5.3 Pulse Width Modulator (PWM)
5.4 Serial Peripheral Interface (SPI)
5.5 Universal Asynchronous Receiver Transmitter (UART)
5.6 Serial Flash (SF) Controller
5.7 Joint Test Action Group (JTAG)
5.8 Real Time Clock (RTC)
5.9 Timer
5.10 Watchdog Timer (WDT)
5.11 Ethernet Media Access Controller (EtherMAC)
5.12 Universal Serial Bus 2.0 (USB 2.0)
5.13 Motor Controller (MC)
5.14 Successive Approximation Register Analog-to-Digital Converter (SAR ADC)
5.15 RF Serial Peripheral Interface Bus (SPI)

5.1 General Purpose Input/Output (GPIO)

The general-purpose input/output (GPIO) is used to transmit the signal between systems and devices. GPIO pins can be configured as input, output, or interrupt input. As an output, state driven on the output pin is controlled by writing the internal register. As an input, the state of the input is detectable by reading the state of an internal register. The GPIO supports the rising edge, falling edge, both-edges, and high level/low level interrupt sense types. The SN93700 Series provides 21 GPIO pins in pinmux architecture. Each pin can be configured as GPIO by the settings as listed in Table 5–1. The base address of GPIO controller is 0x92B0_0000.

Table 5–1 List of GPIOs

GPIO	Location	Note
GPIO[13:0]	Set by upper level pinmux (refer to section 0)	Upper level pinmux
GPIO14	SEN_GPIO0	1.8V or 3.3V variable IO
GPIO15	SEN_GPIO1	1.8V or 3.3V variable IO
GPIO16	TRSTN when JTAG_EN = 1	JTAG pin
GPIO17	TCK when JTAG_EN = 1	JTAG pin
GPIO18	TMS when JTAG_EN = 1	JTAG pin
GPIO19	TDI when JTAG_EN = 1	JTAG pin
GPIO20	TDO when JTAG_EN = 1	JTAG pin

Features of the GPIO include:

- Each pin triggers the GPIO interrupt independently
- The interrupt generation of each pin is triggered by rising/falling edge, both edges, or high/low level
- Pull high or low is possible for each pin
- De-bounce function for each pin
- Output data bit be set or cleared independently
- All pins are set to the input mode at hardware reset
- Partial GPIO pins with variable voltage level of 1.8V or 3.3V.

The GPIO peripheral generates CPU interrupts and DMA events in different interrupt/event generation modes while providing generic connections to external devices.

5.1.1 Register Summary

Table 5–2 Registers of GPIO

Address ranges: 0x92B0_0000 to 0x92BF_FFFF

Offset	Description
0x00000	GPIO data output
0x00004	GPIO data input
0x00008	GPIO direction
0x0000C	GPIO bypass mode
0x00010	GPIO output bit set
0x00014	GPIO output bit clear
0x00018	GPIO pull-up
0x0001C	GPIO pull-level
0x00020	GPIO interrupt enable
0x00024	GPIO interrupt status
0x00028	GPIO masked interrupt status
0x0002C	GPIO interrupt mask
0x00030	GPIO interrupt clear.
0x00034	GPIO interrupt trigger mode (edge/level)
0x00038	GPIO interrupt trigger type (single/both edge)
0x0003C	GPIO interrupt trigger polarity (rising/falling/high/low)
0x00040	GPIO de-bouncing enable
0x00044	GPIO de-bouncing control
0x00048–0xFFFFC	Reserved

5.1.2 Timing

The table below lists switching characteristics over recommended operating conditions for GPIO.

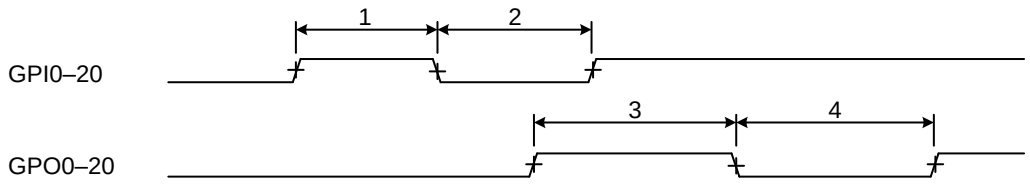


Figure 5–1 GPIO Port Timing

Table 5–3 Switching Characteristics for GPIO Outputs

No.	Parameter		Device[25]		Unit
			MIN.	MAX.	
1	$t_{w(GPIH)}$	Pulse duration, GPI0–20 high	1 PCLK cycle[26]	–	ns
2	$t_{w(GPIL)}$	Pulse duration, GPI0–20 low	1 PCLK cycle[26]	–	ns
3	$t_{w(GPOH)}$	Pulse duration, GPO0–20 high	1 PCLK cycle[26]	–	ns
4	$t_{w(GPOL)}$	Pulse duration, GPO0–20 low	1 PCLK cycle[26]	–	ns

[25] The parameter value should not be used as a maximum performance specification. Actual performance of back-to-back accesses of the GPIO is dependent upon internal bus activity.
[26] Peripheral clock (PCLK) cycle = APB clock period

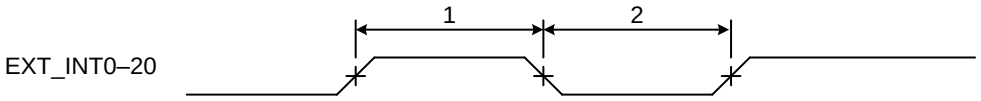


Figure 5–2 GPIO External Interrupt

5.2 Inter-integrated Circuit (I²C)

The inter-integrated circuit (I²C) interface implements the standard I²C master/slave functions and complies with the Philips I²C bus protocol. It serves as a standard master I²C device to receive/transmit data from/to a slave device over the I²C bus. On the contrary, it can also serve as a slave to respond to requests. The I²C is a two-wire bi-directional serial bus that provides a simple and efficient method of data exchange while minimizing the interconnection requirements between devices. The I²C interface is mainly used for controlling external I²C devices.

The SN93700 Series I²C is allowed to communicate with external I²C devices. The interface has two pins, serial clock (SCL) and serial data (SDA). It supports bit rates of up to 400 kbps. The SN93700 Series I²C has two sets of I²C controllers. The first set has two I²C pins and is at base address 0x9240_0000. The second instance has five pins including one SCL pin and four SDA pins for time sharing to control four sets of I²C, and is at offset 0xA8 in the global setting registers and base address 0x9250_0000.

Features of the I²C include:

- Programmable clock division register
- Standard and fast modes up to 400 KHz
- 7-bit, 10-bit, and general call addressing modes
- Glitch suppression throughout the de-bounce circuits
- Programmable slave address
- Master-transmit, master-receive, slave-transmit, and slave-receive modes
- Slave mode general call address detection
- Optional open-drain, push-pull or GPIO (internal level pinmux) modes
- Upper level pinmux options

5.2.1 Register Summary

Table 5–4 Registers of I²C

Address ranges: 0x9240_0000 to 0x924F_FFFF and 0x9250_0000 to 0x925F_FFFF

Offset	Description
0x00000	I²C control
0x00004	I²C status
0x00008	I²C clock division
0x0000C	I²C data
0x00010	I²C slave address
0x00014	I²C glitch suppression control
0x00018	I²C bus monitor
0x0001C	I²C GPIO mode control
0x00020–0x0002C	Reserved
0x00030	I²C version
0x00034	I²C multi-master mode
0x00038–0xFFFFC	Reserved

5.2.2 I²C Internal Pinmux

The I²C pins have two pinmux levels. The internal pinmux option of I2C1_SCL, I2C1_SDA, I2C2_SCL, I2C2_SDA0, I2C2_SDA1, I2C2_SDA2, and I2C2_SDA3 is GPIO (pin type: I/O). For upper level pinmux options, see Table 2–16.

5.2.3 Clock Ratios and Timing

According to the standard I²C protocol, the start signal, Start, is a special signal sent by the master on the bus to wake up all the slaves and indicates start of a data transfer. The slave address transmit (slave address + W/R) refers to the first data packet sent by the master after a start condition. It has seven slave address bits and one read/write bit. The equation for clock ratios is:

SCLout = PCLK / [2 x (SCL_COUNT + 2) + GSR]

(Max *SCLout* is up to 400K, SCL_COUNT > 3 + GSR + TSR)

Two data packets need to be transmitted only when it is a 10-bit slave address. Otherwise, other bits (except the 10 bits address) are reserved according to the protocol. Each slave is used to transmit or receive data based on the address information. After receiving the slave address successfully, the corresponding slave pulls down the SDA at the ninth SCL cycle and returns an acknowledgement signal (ACK) to the master. Then, a subsequent data transfer can start. The data transfer "DATA" refers to data receive/transmit according to read/write commands after the master receives the slave address ACK signal successfully. During the data transfer, the SDA changes its state only when the SCL is low. The SDA holds when the SCL is high. Each time the receiver gets one byte, it must send an ACK signal to the transmitter. The transmitter stops or restarts the data transfer when it does not receive the ACK signal.

The stop signal, Stop, is a special signal sent by the master to indicate the end of the data transfer according to the I²C protocol. It occurs when the transfer is complete and there are no subsequent transfers required. Once the master sends the stop signal, the slave must release the bus.

Table 5–5 Timing Requirements for I²C

No.	Parameter		Device				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
1	$t_{c(SCL)}$	Cycle time, SCL	10	–	2.5	–	µs
2	$t_{su(SCLH-SDAL)}$	Setup time, SCL high before SDA low (for a repeated START condition)	4.7	–	0.6	–	µs
3	$t_{h(SCLL-SDAL)}$	Hold time, SCL low after SDA low (for a START and a repeated START condition)	4	–	0.6	–	µs
4	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7	–	1.3	–	µs
5	$t_{w(SCLH)}$	Pulse duration, SCL high	4	–	0.6	–	µs
6	$t_{su(SDAV-SCLH)}$	Setup time, SDA valid before SCL high	250	–	100	–	µs
7	$t_{h(SDA-SCLL)}$	Hold time, SDA valid after SCL low	0	3.45	0	0.9	µs
8	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7	–	1.3	–	µs
9	$t_{r(SDA)}$	Rise time, SDA	–	1000	$20 + 0.1C_b$[27]	300	ns
10	$t_{r(SCL)}$	Rise time, SCL	–	1000	$20 + 0.1C_b$[27]	300	ns
11	$t_{f(SDA)}$	Fall time, SDA	–	300	$20 + 0.1C_b$[27]	300	ns
12	$t_{f(SCL)}$	Fall time, SCL	–	300	$20 + 0.1C_b$[27]	300	ns
13	$t_{su(SCLH-SDAH)}$	Setup time, SCL high before SDA high (for STOP condition)	4	–	0.6	–	µs
14	$t_{w(SP)}$	Pulse duration, spike (must be suppressed)	–	–	–	50	µs
15	C_b[16]	Capacitive load for each bus line	–	400	–	400	pF

[27] Cb = total capacitance of one bus line in pF. Faster fall-times are allowed when mixing with HS-mode devices.

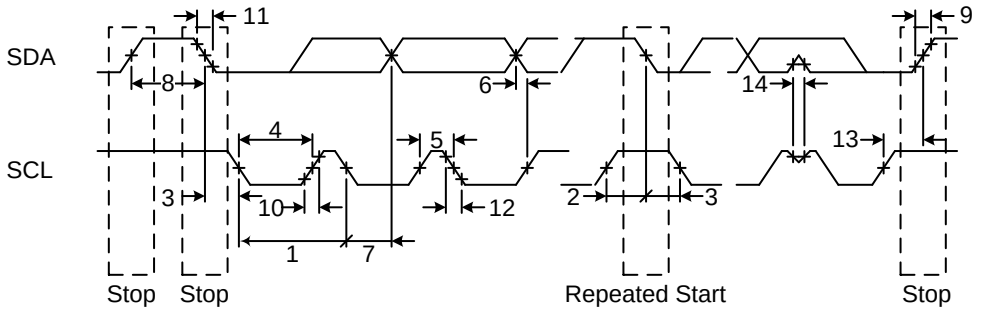


Figure 5–3 I²C Receive Timings

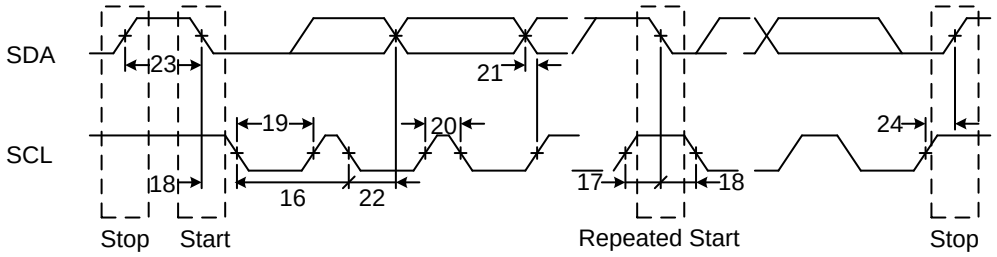


Figure 5–4 I²C Transmit Timings

Table 5–6 Switching Characteristics for I²C

No.	Parameter		Device				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
16	$t_{c(SCL)}$	Cycle time, SCL	10	–	2.5	–	µs
17	$t_{d(SCLH-SDAL)}$	Delay time, SCL high to SDA low (for a repeated START condition)	4.7	–	0.6	–	µs
18	$t_{d(SDAL-SCLL)}$	Delay time, SDA low to SCL low (for a START and a repeated START condition)	4	–	0.6	–	µs
19	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7	–	1.3	–	µs
20	$t_{w(SCLH)}$	Pulse duration, SCL high	4	–	0.6	–	µs
21	$t_{d(SDAV-SCLH)}$	Delay time, SDA valid to SCL high	250	–	100	–	µs
22	$t_{v(SCLL-SDAV)}$	Valid time, SDA valid after SCL low (For I²C devices)	0	–	0	0.9	µs
23	$t_{w(SDAH)}$	Pulse duration, SDA high between STOP and START conditions	4.7	–	1.3	–	µs
24	$t_{d(SCLH-SDAH)}$	Delay time, SCL high to SDA high (for STOP condition)	4	–	0.6	–	µs
25	C_p	Capacitance for each I²C pin	–	10	–	10	µs

5.3 Pulse Width Modulator (PWM)

The pulse width modulator (PWM) is very common in embedded systems. The PWM provides the method to generate a pulse periodic waveform for motor control or can act as a digital-to-analog converter with some external components. The PWM peripheral is basically a timer with a period

counter and a duration comparator where the period and pulse duration are both programmable. There are 16 PWM outputs with upper level pinmux option of GPIO. The PWM is in base address 0x9040_0000.

Features of the PWM include:

- Control Iris, IR LED, and status LED
- The formula of PWM Period TPeriod is:

Tbase = 96 MHz x (PWMn_RATE)
TPeriod = Tbase x (PWMn_PERIOD)
Tduty = Tbase x PWMn_HIGH_CNT

Range of PWMn_RATE is from 1 to 127.
Range of PWMn_PERIOD is from 1 to 4096.
Range of PWMn_HIGH_CNT is from 0 to 4096.

- Upper level pinmux options

5.3.1 Register Summary

Table 5–7 Registers of PWM

Address ranges: 0x9040_0000 to 0x9040_FFFF

Offset	Description
0x00000	PWM enable
0x00004–0x00040	PWM period and duty
0x00044–0x00050	PWM rate
0x00054–0xFFFFFC	Reserved

5.3.2 PWM Pinmux

Pinmux of PWM is in the upper level, refer to Table 2–16 for mapping.

5.3.3 Timing

The table below lists switching characteristics over recommended operating conditions for PWM outputs.

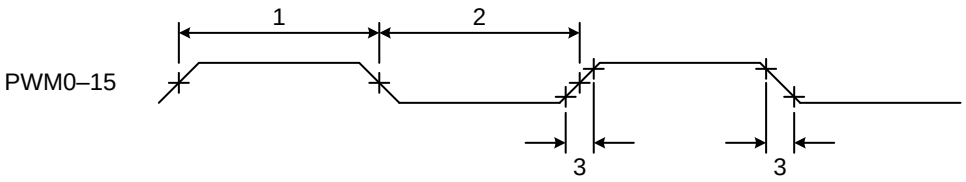


Figure 5–5 PWM Output Timing

Table 5–8 Switching Characteristics for PWM Outputs

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{w(PWMH)}$	Pulse duration, PWM high	1 PCLK cycle[26]	–	ns
2	$t_{w(PWML)}$	Pulse duration, PWM low	1 PCLK cycle[26]	–	ns
3	$t_{t(PWM)}$	Transition time	–	5	ns

5.4 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) bus is a synchronous serial data link standard with 4-wire serial bus. The frame format of the SN93700 Series SPI complies with the frame format of Motorola's SPI. It operates with a single master device or one/more slave devices. The SPI is in base address 0x9200_0000.

Features of the SPI include:

- The read/write data/command interface is compliant with AMBA APB bus 2.0
- Master and slave modes
- Internally or externally controlled serial bit clock
- Programmable serial bit clock polarity, phase, and frequency
- Programmable serial bit data sequence (MSB or LSB first)
- Internal level pinmux GPIO mode
- Upper level pinmux options

When the SPI is in master mode, it has to connect with one slave device as shown in Figure 5–6.

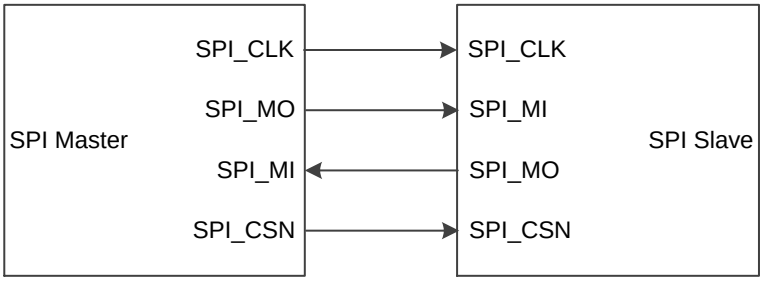


Figure 5–6 SPI Connection Diagram

5.4.1 Register Summary

Table 5–9 Registers of SPI

Address ranges: 0x9200_0000 to 0x920F_FFFF

Offset	Description
0x00000	SPI control 0
0x00004	SPI control 1
0x00008	SPI control 2
0x0000C	SPI status
0x00010	SPI interrupt control
0x00014	SPI interrupt status
0x00018	SPI data
0x0001C	Reserved
0x00020	AC-link slot valid
0x0001C–0x0003C	Reserved
0x00040	SPI version
0x00044	SPI feature
0x00048–0xFFFFC	Reserved

5.4.2 Clock Ratios and Timing

When the SPI controller is in master mode, the frequency of SCLK_OUT is derived from the following equation:

Fsclk = Fspiclk[28] / (2 x (SCLKDIV + 1))

The bit rate of SPI is the frequency of the SCLK_OUT which is controlled by SPI_SCLKDIV in the control register. When the SPI controller is in slave mode, SCLKDIV is ignored, and the SPI transfer bitrate is decided on the master side. Due to clocks synchronization, the bit clock from the master side has to be slower than SPICLK by at least six times.

SCLK stops toggling when it is idling. The frame/sync is used as the chip-select signal. Through the SPI interface, data is transmitted and received simultaneously to and from an external device. The data lines are synchronized by a serial clock.

In master mode, when the SPI controller is enabled and TX FIFO contains data, the transmit logic reads the data in TX FIFO and shifts it out at every transmit edge (depending on SCLKPO and SCLKPH) from MSB to LSB. Synchronously, the receive logic receives data. After the LSB is transmitted or received, frame/sync holds low for half or one SCLK cycle, depending on SCLKPH, and then pulled high if TX FIFO is empty. Received data is written into RX FIFO. When TX FIFO is not empty, the transmit logic restarts to transmit data.

In slave mode, when frame/sync is activated and SCLK is enabled, the transmit logic tries to shift the data into the TX FIFO even if the TX FIFO is empty. The transmit FIFO under-run interrupt is issued when TX FIFO is enabled. The receive logic receives data at the same time, and the data is written into RX FIFO.

[28] Fspiclk = PCLK

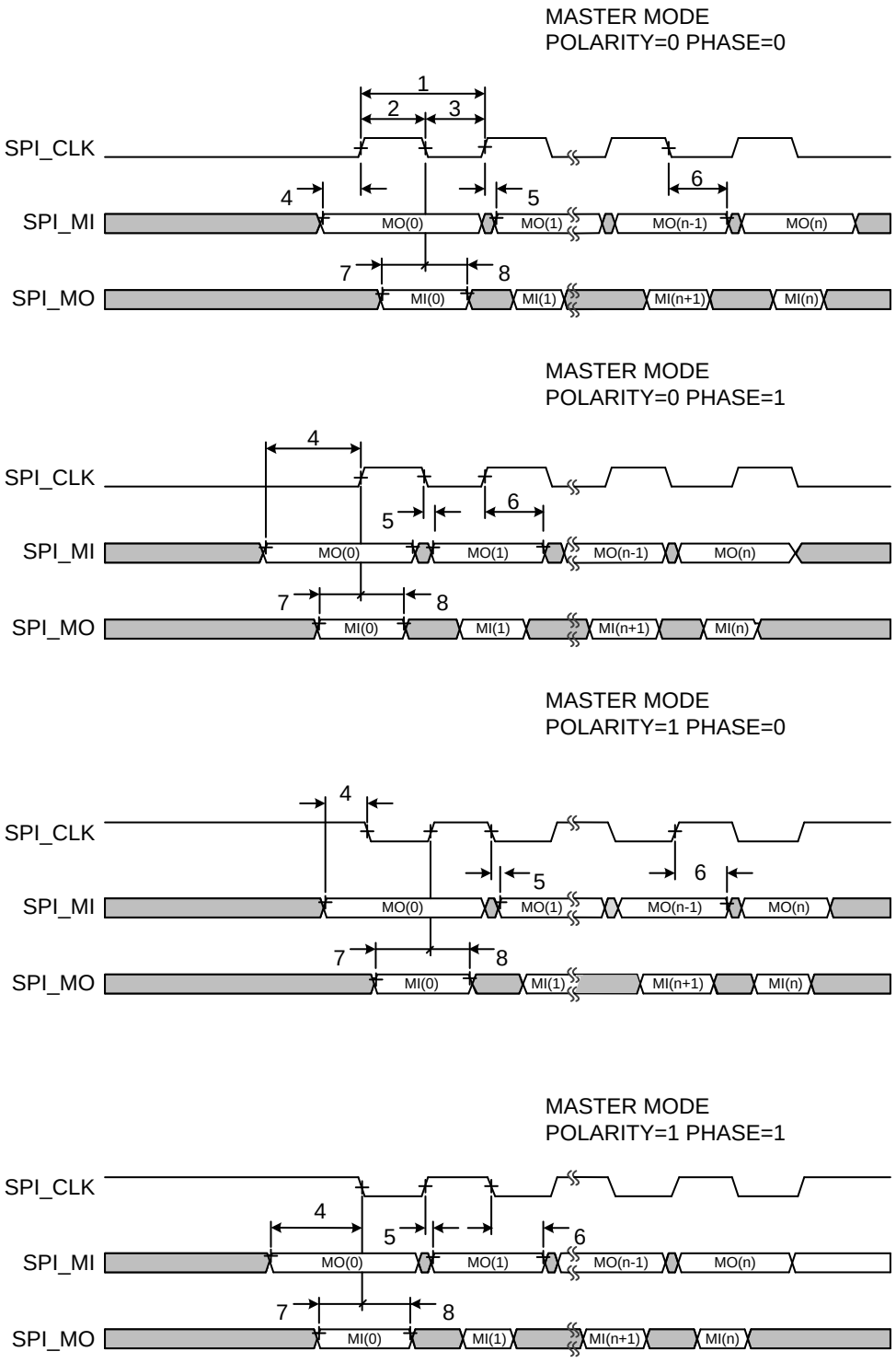


Figure 5–7 SPI Master Mode Timings

Table 5–10 Switching Characteristics for SPI in Master Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{c(CLK)}$	Cycle time, SPI_CLK	2 PCLK cycles[26]	131072 PCLK cycles[26]	ns
2	$t_{w(CLKH)}$	Pulse width, SPI_CLK high	0.45 ($t_{c(CLK)}$)	–	ns
3	$t_{w(CLKL)}$	Pulse width, SPI_CLK low	0.45 ($t_{c(CLK)}$)	–	ns
4	$t_{osu(TX-CLK)}$	Ouput setup time, SPI_MI valid before initial SPI_CLK rising or falling edge.	0.5 ($t_{c(CLK)}$) - 3	–	ns
5	$t_{d(CLK-TX)}$	Delay time, SPI_CLK transmit rising or falling edge to SPI_MI output	-3	3	ns
6	$t_{oh(CLK-TX)}$	Output hold time, SPI_MI valid after receive rising or falling edge of SPI_CLK	0.5 ($t_{c(CLK)}$) - 3	–	ns

Table 5–11 Input Timing Requirements for SPI in Master Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
7	$t_{su(RX-CLK)}$	Setup time, SPI_MO valid before receive rising or falling edge of SPI_CLK	4	–	ns
8	$t_{h(CLK-RX)}$	Hold time, SPI_MO valid after receive rising or falling edge of SPI_CLK	4	–	ns

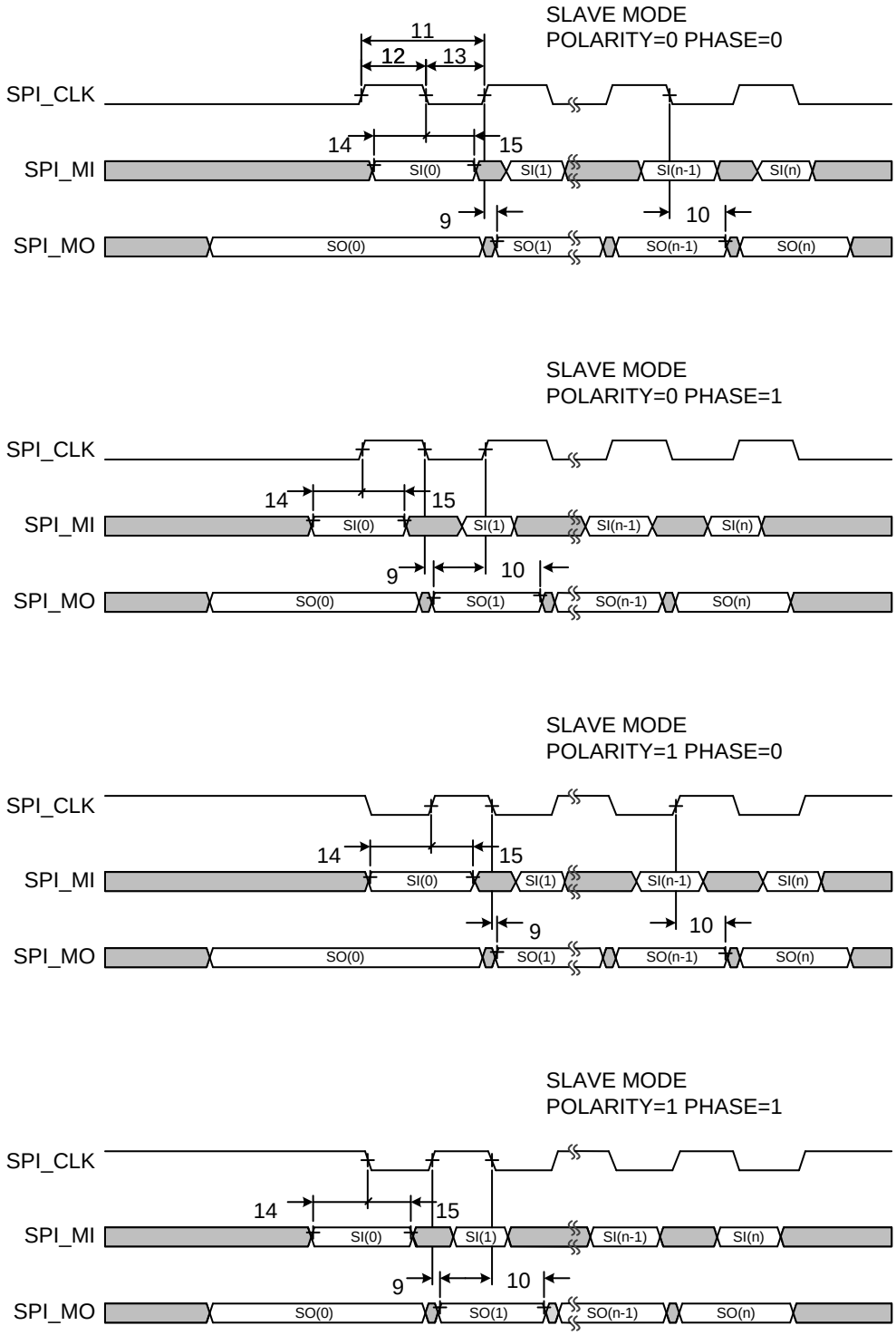


Figure 5–8 SPI Slave Mode Timings

Table 5–12 Switching Characteristics for SPI in Slave Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
9	$t_{d(CLK-TX)}$	Delay time, transmit rising or falling edge of SPI_CLK to SPI_MI output valid	2	8	ns
10	$t_{oh(CLK-TX)}$	Output hold time, SPI_MI valid after receive rising or falling edge of SPI_CLK	4	–	ns

Table 5–13 Input Timing Requirements for SPI in Slave Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
11	$t_{c(CLK)}$	Cycle time, SPI_CLK	6 PCLK cycles[26]	–	ns
12	$t_{w(CLKH)}$	Pulse width, SPI_CLK high	0.45 ($t_{c(CLK)}$)	–	ns
13	$t_{w(CLKL)}$	Pulse width, SPI_CLK low	0.45 ($t_{c(CLK)}$)	–	ns
14	$t_{su(RX-CLK)}$	Setup time, SPI_MO valid before receive rising or falling edge of SPI_CLK	4	–	ns
15	$t_{h(RX-CLK)}$	Setup time, SPI_MO valid after receive rising or falling edge of SPI_CLK	4	–	ns

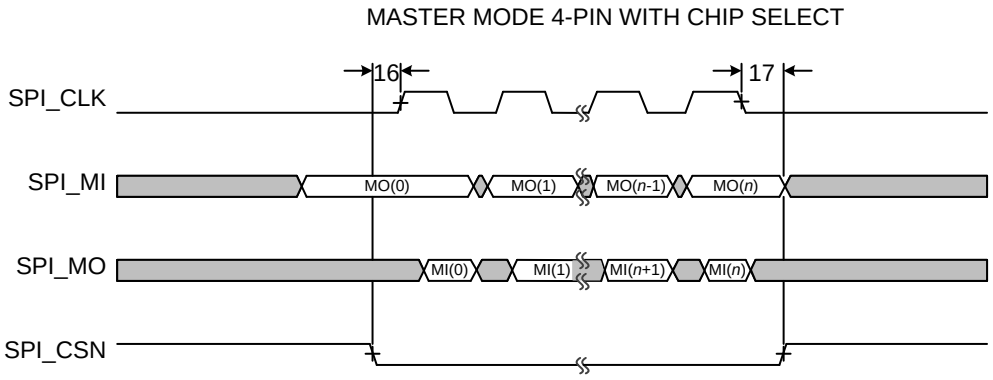


Figure 5–9 SPI Master Mode Timing (4-pin)

Table 5–14 Output Switching Characteristics of 4-pin Chip-select Option in Master Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
16	$t_{osu(TX-CLK)}$	Output setup time, SPI_CSN active before initial SPI_CLK rising or falling edge.	$t_{c(CLK)}$ - 4	$t_{c(CLK)}$ + 4	ns
17	$t_{d(CLK-TX)}$	Delay time, final SPI_CLK falling or rising edge to master de-asserting SPI_CSN	0.5 ($t_{c(CLK)}$) - 4	0.5 ($t_{c(CLK)}$) + 4	ns

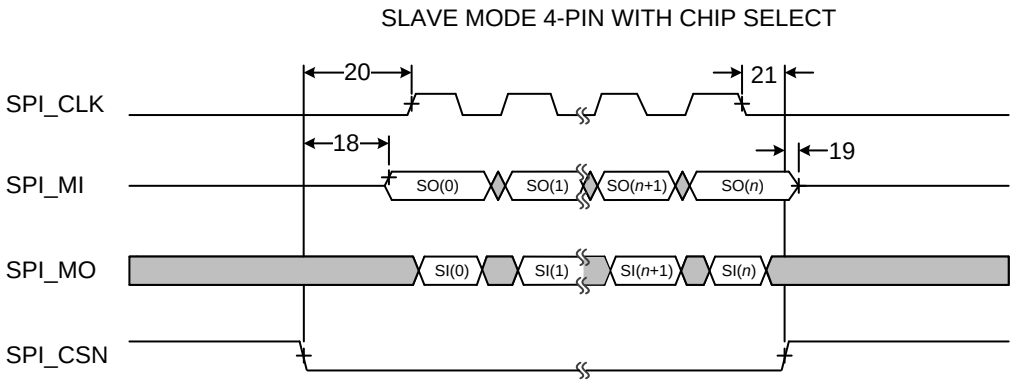


Figure 5–10 SPI Slave Mode Timing (4-pin)

Table 5–15 Output Switching Characteristics of 4-pin Chip-select Option in Slave Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
18	$t_{d(FSL-TX)}$	Delay time, master asserting SPI_CSN to slave driving SPI_MI.	–	3 PCLK cycles[26] + 13	ns
19	$t_{dis(FSH-TX)}$	Disable time, master deasserting SPI_CSN to slave driving SPI_MI high impedance.	–	3 PCLK cycles[26] + 13	ns

Table 5–16 Additional Input Timing Requirements of 4-pin Chip-select Option in Slave Mode

No.	Parameter		Device[26]		Unit
			MIN.	MAX.	
20	$t_{su(FSL-CLK)}$	Setup time, SPI_CSN asserted at slave to first SPI_CLK edge (rising or falling) at slave	3 PCLK cycles[26]	–	ns
21	$t_{d(CLK\overline{\ }FSH)}$	Delay time, final falling edge SPI_CLK to SPI_CSN deasserted.	2 PCLK cycles[26]	–	ns

5.5 Universal Asynchronous Receiver Transmitter (UART)

- The SN93700 Series UART controller uses serial communication for data transmission. The UART module converts the data received from a peripheral device or modem (serial-to-parallel), and data received from the CPU (parallel-to-serial). Each UART includes a programmable baud rate generator capable of dividing the module's reference clock by divisors to generate the correct UART baud rate. The SN93700 Series provides two sets of UART, wherein one supports flow control (CTS/RTS).

  Features of the UART controller include:
  - Baud rates from 317 bps up to 12 Mbps
  - One start bit, 8-bit data, and one or two stop bit format
  - 32 bytes TX and 32 bytes RX FIFO buffer
  - TX and RX ready interrupt
  - CPU access with 8/16/24/32-bit data width
  - AMBA APB DMA with 32-bit data width
  - AMBA APB DMA AHB 2.0 burst 1/4 mode
  - FIFO threshold interrupt more for TX/RX mode
  - Modem flow control function with CTS and RTS
  - Internal level pinmux GPIO mode

- Upper level pinmux options

The SN93700 Series UART limitation:
APB DMA is used in transferring data by programming the UART in DMA mode. Since APB DMA is a 32-bit DMA master, data must be aligned in 32-bit format.

Figure 5–11 is the UART connection diagram with flow control.

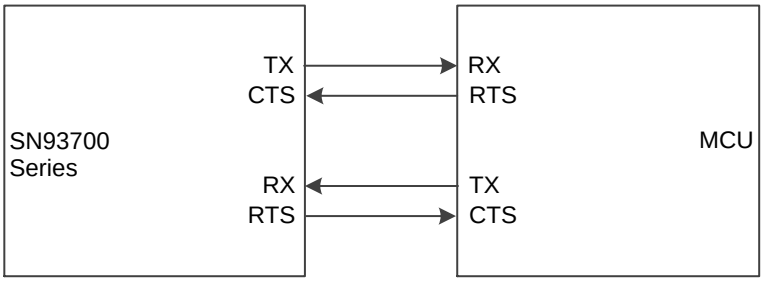


Figure 5–11 UART Connection Diagram

Figure 5–12 is the UART operation diagram with flow control.

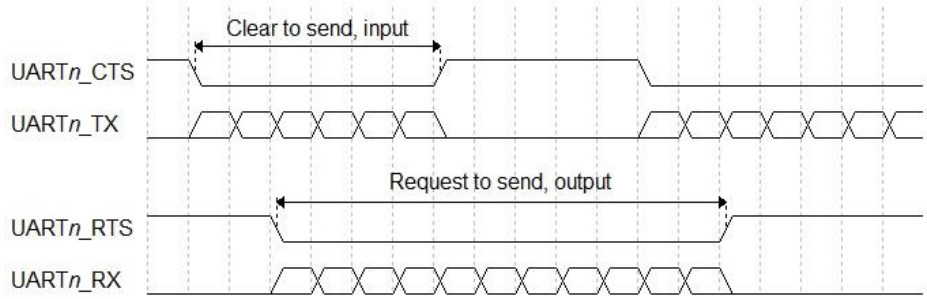


Figure 5–12 UART Operation Diagram

5.5.1 Register Summary

Table 5–17 Registers of UART

Address ranges: 0x9210_0000 to 0x921F_FFFF and 0x9220_0000 to 0x922F_FFFF

Offset	Description
0x00000	UART main function control
0x00004	UART DMA TX size
0x00008	UART DMA RX size
0x0000C	UART baud rate
0x00010	UART data
0x00014	UART GPIO control
0x00018	UART DMA TX/RX FIFO threshold
0x0001C	UART version
0x00020–0xFFFFC	Reserved

5.5.2 Baud Rate, Timing, and Transfer Format

It is required to set the proper baud rate for UART transmission initiation. The calculation of the target baud rate involves two factors. One is a base constant, BASE_FREQ, and the other is a divider, RS_RATE. The formula of the baud rate calculation is:

Baud = *BASE_FREQ* / *RS_RATE*[29] [30]

RS_RATE and TRX_BASE are registers located at offset 0x9210_000C[6:0] and offset 0x9210_000C[11:7] for UART1; offset 0x9220_000C[6:0] and offset 0x9220_000C[11:7] for UART2.

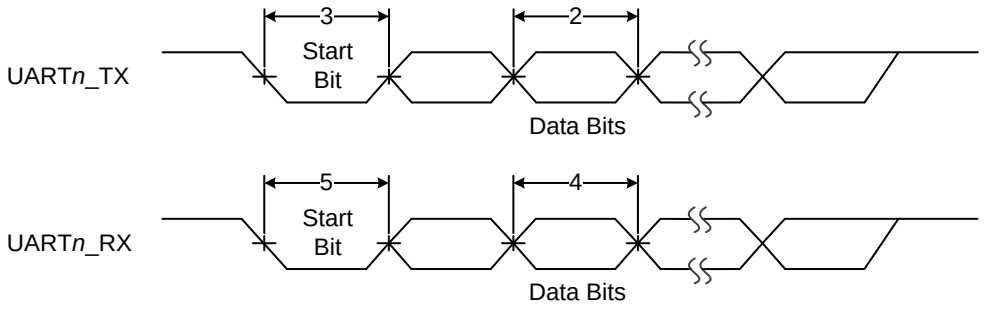


Figure 5–13 UART Transmit/Receive Timing

Table 5–18 Timing Requirements for UART Receiver

No.	Parameter		Device		Unit
			MIN.	MAX.	
4	$t_{w(URXDB)}$	Pulse duration, receive data bit	0.96U[31]	1.05U[31]	ns
5	$t_{w(URXSB)}$	Pulse duration, receive start bit	0.96U[31]	1.05U[31]	ns

The table below lists switching characteristics over recommended operating conditions for the UART transmitter.

Table 5–19 Switching Characteristics for UART Transmitter

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$f_{(baud)}$	UART1 maximum programmable baud rate	0.0004	12	MHz
		UART2 maximum programmable baud rate	0.0004	12	MHz
2	$t_{w(URXDB)}$	Pulse duration, transmit data bit	U[31] – 2	U[31] + 2	ns
3	$t_{w(URXSB)}$	Pulse duration, transmit start bit	U[31] – 2	U[31] + 2	ns

The SN93700 Series UART contains TX, RX, CTS, and RTS pins for transmitting, receiving and flow control. It has one start bit, 8-bit data, and one/two stop bits for each communication.

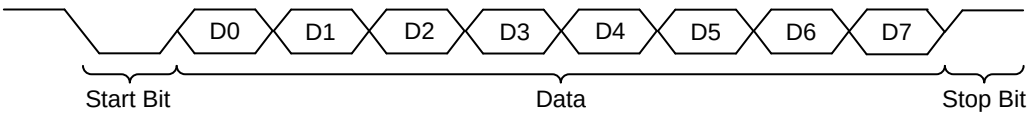


Figure 5–14 UART Transfer Format

[29] BASE_FREQ is a base clock rate close to 12 MHz.
[30] BASE_FREQ = PCLK / 8 / TRX_BASE, where PCLK is fixed to 96 M or 10 MHz clock rate.
[31] U = UART baud time = 1 / programmed baud rate.

5.6 Serial Flash (SF) Controller

Features of the SF controller include:

- Built-in SPI controller
- Multiple DMA block transfers
- Auto multiple block read/write command
- DMA for large data transfers
- Built-in CRC-32/16 for data contents check
- Built-in contents protection function
- Supports MXIC/SST command series serial flash

The serial flash controller block diagram is as shown in Figure 5–15.

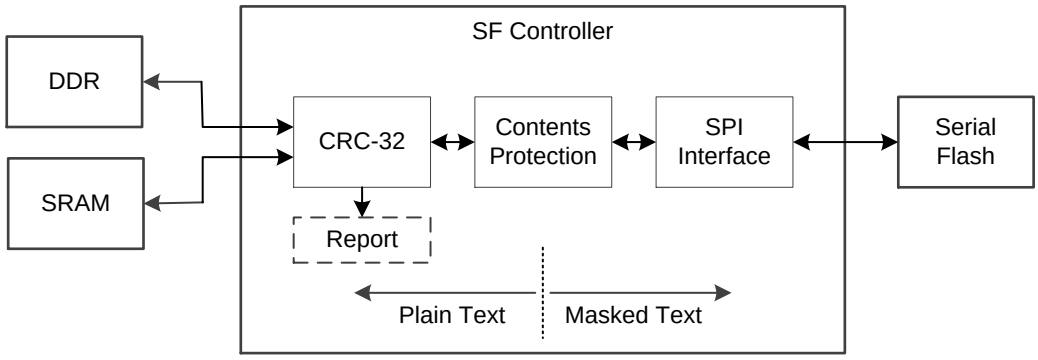


Figure 5–15 SF Controller Block Diagram

5.6.1 Register Summary

Table 5–20 Registers of Serial Flash

Address ranges: 0x9030_0000 to 0x9030_FFFF

Offset	Description
0x00000	Serial Flash controller main function control
0x00004	Serial Flash controller DMA size and operation mode control 1
0x00008	Serial Flash controller CRC-32
0x0000C	Contents protection function control
0x00010	Contents encode engine parameter 1
0x00014	Contents encode engine parameter 2
0x00018	Contents encode engine parameter 3
0x0001C	Contents encode engine parameter 4
0x00020	Serial Flash read/write command set 1
0x00024	Serial Flash read/write command set 2
0x00028	Serial Flash read/write command set 3
0x0002C	Serial Flash controller operation mode control 2
0x00030	Serial Flash controller GPIO mode input value
0x00034	Serial Flash controller GPIO mode output value
0x00038	Serial Flash controller GPIO mode output enable
0x0003C	Serial Flash read/write address
0x00040	CRC32 polynomial parameter
0x00044	CRC order
0x00048	Serial Flash controller M-DMA block number
0x0004C	Serial Flash controller timeout count
0x00050	Serial Flash controller DMA function control and interrupt flags
0x00054–0x00058	Reserved
0x0005C	Serial Flash controller DMA start address
0x00060–0x0006C	Reserved
0x00070–0x0007C	Serial Flash controller read/write data
0x00080	Serial Flash controller version

Offset	Description
0x00084–0x0FFFC	Reserved

5.6.2 Timing

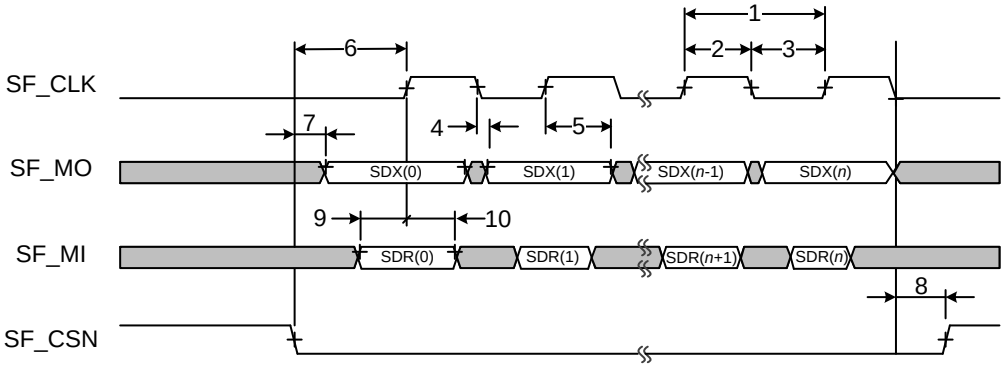


Figure 5–16 SF Master Mode Input Timing

Table 5–21 Switching Characteristics for SF Controller

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{c(CLK)}$	Cycle time, SF clock	20.83	2676.9	ns
2	$t_{w(CLKH)}$	Pulse width, SF clock high	9	11	ns
3	$t_{w(CLKL)}$	Pulse width, SF clock low	9	11	ns
4	$t_{d(CLK-SDX)}$	Delay time, SF clock transmit falling edge to SF_MO data output	-3.5	-1	ns
5	$t_{oh(CLK-SDX)}$	Output hold time, SF_MO data valid after receive rising edge of clock	6.5	–	ns
6	$t_{d(CSN-CLK)}$	Delay time, SF chip select asserting to the first SF clock rising edge	39	–	ns
7	$t_{d(CSN-SDX)}$	Delay time, SF chip select asserting to SF_MO data valid	17	–	ns
8	$t_{d(CLK-CSN)}$	Delay time, the final SF clock falling edge to SF chip select de-asserting	19	–	ns

Table 5–22 Input Timing Requirements of SF Controller in Master Mode

No.	Parameter		Device		Unit
			MIN.	MAX.	
9	$t_{su(SDR-CLK)}$	Setup time, SF_MI data valid before receive rising edge of SF clock	0.25	–	ns
10	$t_{h(CLK-SDR)}$	Hold time, SF_MI data valid after receive rising edge of SF clock	6.5	–	ns

5.7 Joint Test Action Group (JTAG)

The JTAG interface is for device emulation. While RST initializes the device, the emulation logic of the device gets initialized too. Only RST has to be released for the device to boot properly. TRSTN may be asserted indefinitely for normal operation, keeping the JTAG port interface and device's emulation logic in the reset state. TRSTN only has to be released when debugging the device with a JTAG controller.

For maximum reliability, an external pull-down is suggested on the TRST pin to prevent TRSTN in an unknown state upon power up.

5.7.1 Register Summary

JTAG I/O controller registers are in offset 0x000A8 of Global Settings as shown in Table 3–1.

5.7.2 Timing

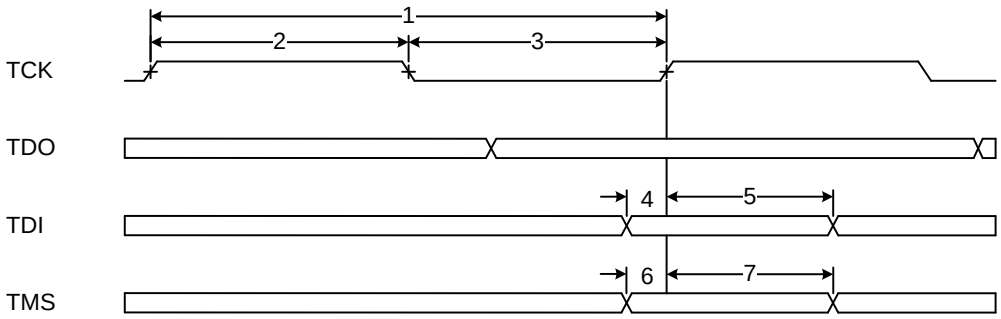


Figure 5–17 JTAG Input Timing

Table 5–23 Timing Requirements for JTAG Test Port

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{c(TCK)}$	Cycle time, TCK	62	–	ns
2	$t_{w(TCKH)}$	Pulse duration, TCK high	29	–	ns
3	$t_{t(TCKLCKL)}$	Transition time, TCK low	29	–	ns
4	$t_{su(TDIV-TCKH)}$	Setup time, TDI valid before TCK high	10	–	ns
5	$t_{h(TCKH-TDIV)}$	Hold time, TDI valid after TCK high	1	–	ns
6	$t_{su(TMSV-TCKH)}$	Setup time, TMS valid before TCK high	10	–	ns
7	$t_{h(TCKH-TMSV)}$	Hold time, TDI valid after TCK high	1	–	ns

The table below lists switching characteristics over recommended operating conditions for the JTAG test port.

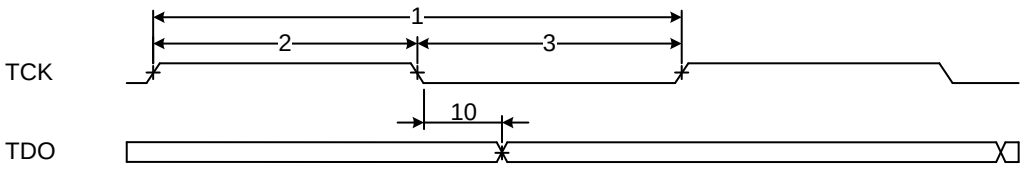


Figure 5–18 JTAG Output Timing

Table 5–24 Switching Characteristics for JTAG Test Port

No.	Parameter		Device		Unit
			MIN.	MAX.	
8	$t_{r(TDO)}$	Rise time, TDO	–	5	ns
9	$t_{f(TDO)}$	Fall time, TDO	–	5	ns
10	$t_{d(TCK-TDOV)}$	Delay time, TCK low to TDO valid	0	25	ns

5.8 Real Time Clock (RTC)

The SN93700 Series real-time clock (RTC) is a flexible, low-area and low-power device. The RTC clock frequency is 32768 Hz. The RTC can keep on counting when the system has been switched to sleep mode. This mechanism guarantees the lowest power consumption no matter the system goes into sleep mode or not. In addition, the RTC provides a programmable auto-alarm function. By using this function, the interrupt will be triggered on each second. The auto-alarm function period can be up to hours. The RTC also provides a programmable wake-up function. By using this function, the interrupt will be triggered at each 1/128 second.

There is a special RTC power domain data with a total data size of 80 bits. The data is kept using RTC power and is kept alive when the system is powered down. Applications can use this data buffer under warm reset to pass information after system reboot. This data buffer is usually used to determine the cause of a system reboot.

Features of the RTC include:

- 30-bit timer, add one per second for the count range from 0 to 1073741823 second, year, month, date, hours, minutes, and seconds used for F/W transfer
- 30-bit alarm timer, add one per second, for interrupts and flags
- 24-bit wakeup timer, add by one per 1/128 second, for interrupts and flags
- Ten banks of RTC power domain data, each data includes 8 bits

Restrictions of the RTC module include:

- At least 1 µs lag between reading from or writing to the RTC register.
- It takes two reads to access the RTC register map offset between 0x00000 and 0x00034
- 32768 Hz crystal must be mounted on a PCB to find the register value of RTC_WR_RDY

Notice for wakeup timer:

- The wakeup time T cannot be 1.
- The first wakeup period is between ***(7.8 ms x (T - 1.5))*** and ***(7.8 ms x (T - 0.5))***, and ***(7.8 ms x T)*** for others.
- When the wakeup time T is 0, the wakeup period is 7.8 ms x 224.

5.8.1 Register Summary

Table 5–25 Registers of RTC

Address ranges: 0x9003_0000 to 0x9003_FFFF

Offset	Description
0x00000	RTC timer value (byte 0)
0x00004	RTC timer value (byte 1)
0x00008	RTC timer value (byte 2)
0x0000C	RTC timer value (byte 3)
0x00010	RTC alarm timer value (byte 0)
0x00014	RTC alarm timer value (byte 1)
0x00018	RTC alarm timer value (byte 2)
0x0001C	RTC alarm timer value (byte 3)
0x00020	RTC wakeup timer value (byte 0)
0x00024	RTC wakeup timer value (byte 1)
0x00028	RTC wakeup timer value (byte 2)
0x0002C	RTC main function control
0x00030	RTC GPIO mode control
0x00034	RTC GPIO mode CTRL enable

Offset	Description
0x00038	RTC password 1
0x0003C	RTC password 2
0x00040	RTC data buffer read/write value (byte 0)
0x00044	RTC data buffer read/write value (byte 1)
0x00048	RTC data buffer read/write value (byte 2)
0x0004C	RTC data buffer read/write value (byte 3)
0x00050	RTC data buffer read/write value (byte 4)
0x00054	RTC data buffer read/write value (byte 5)
0x00058	RTC data buffer read/write value (byte 6)
0x0005C	RTC data buffer read/write value (byte 7)
0x00060	RTC data buffer read/write value (byte 8)
0x00064	RTC data buffer read/write value (byte 9)
0x00068–0x000FC	Reserved
0x00100	RTC status
0x00104–0x0FFFC	Reserved

5.9 Timer

The SN93700 Series provides three sets of timers. Each timer can be divided into three independent sets of sub-timers. Each sub-timer uses the system clock for either increment or decrement counting. Two matching registers are provided for each sub-timer. Whenever a value of the matching registers equals to the sub-timer increment or decrement counting value, timer interrupt is triggered. Once the overflow occurs, the timer interrupt is controlled by the register setting. The timers are at base address 0x92C0_0000, 0x92D0_0000, and 0x92E0_0000.

Features of the timers include:

- Three independent 32-bit timer programming models
- Interrupts issued upon the overflow and time-up
- Each sub-timer has two match registers
- Programmable decrementing or incrementing modes on the counter

5.9.1 Register Summary

Table 5–26 Registers of Timer

Address ranges: 0x92C0_0000 to 0x92CF_FFFF, 0x92D0_0000 to 0x92DF_FFFF, and 0x92E0_0000 to 0x92EF_FFFF

Offset	Description
0x00000	Timer 1 counter
0x00004	Timer 1 auto reload value
0x00008	Timer 1 match value
0x0000C	Timer 1 match value
0x00010	Timer 2 counter
0x00014	Timer 2 auto reload value
0x00018	Timer 2 match value
0x0001C	Timer 2 match value
0x00020	Timer 3 counter
0x00024	Timer 3 auto reload value
0x00028	Timer 3 match value
0x0002C	Timer 3 match value
0x00030	Timer 1/2/3 control registers
0x00034	Interrupt status register
0x00038	Interrupt mask register
0x0003C–0xFFFFC	Reserved

5.10 Watchdog Timer (WDT)

The watchdog timer (WDT) is a safeguard system operation that prevents system lock up. There are two WDTs with a dedicated ILRC@32.768KHz, one for time-out reset (default enabled for 15 sec.) and

one for time-out interrupt. In normal operation, the software must reload the WDT periodically to prevent the watchdog counter from under-flowing (decremented to zero). The WDT generates one or a combination of the following signals: reset, interrupt, or external interrupt signal.

Features of the WDT include:

- 32-bit watchdog counter
- Counter restart
- Generate reset signals
- Watchdog timer clock from 32.768 KHz ILRC
- Programmable assert duration of WD_RST, WD_INTR, and WD_EXT
- Generate interrupts to the system

5.10.1 Register Summary

Table 5–27 Registers of WDT

Address ranges: 0x92C0_0000 to 0x92CF_FFFF, 0x92D0_0000 to 0x92DF_FFFF, and 0x92E0_0000 to 0x92EF_FFFF

Offset	Description
0x00000	WDT counter
0x00004	WDT auto reload value
0x00008	WDT restart
0x0000C	WDT control
0x00010	WDT status
0x00014	WDT clear
0x00018	WDT interrupt pulse width
0x0001C–0xFFFFC	Reserved

5.11 Ethernet Media Access Controller (EtherMAC)

The Ethernet Media Access Controller (EtherMAC) provides an efficient interface between the device and a network. It includes a DMA engine, on-chip memory (TX FIFO and RX FIFO), and supports both 10Base-TX (10 Mbps) and 100Base-TX (100 Mbps) in either half-duplex or full-duplex mode with reduced media independent interface (RMII)[32]. The frequencies supported for transmitting and receiving clocks are fixed at 50 MHz for both 10 Mbps and 100 Mbps. The EtherMAC handles the flow of packet data between the device and the PHY. The MDIO module controls PHY configuration and status monitoring. The EtherMAC module is fully compliant with the IEEE 802.3 standard, describing the “carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer” specifications.
The SN93700 Series provides a high quality 10/100M EtherMAC including, DMA engine, on-chip memory (TX FIFO and RX FIFO), and RMII interface. The EtherMAC provides the capability of the AHB master and full compliance with IEEE 802.3 100 Mb/s and 10 Mb/s specification with RMII interface. The DMA engine handles all the data transfers between the system memory and the on-chip memory to reduce the CPU loading, maximizing the performance and minimizing the size of FIFO requirements. The EtherMAC has an internal FIFO buffer, so there is no requirement for external memory. The RMII interface supports two specific data rates, 10 Mbps and 100 Mbps.

Features of the EtherMAC include:

- DMA engine for transmitting and receiving packets
- Zero-copy data transfer
- Programmable AHB burst size
- Transmit and receive interrupt mitigation
- Contains independent TX/RX FIFOs (2 KB each)
- Half-duplex and full-duplex modes
- Flow control for full-duplex and backpressure for half-duplex

[32] The standard 802.3 media independent interface (MII) is ***not*** available.

5.11.1 Register Summary

Table 5–28 Registers of EtherMAC

Address ranges: 0x9450_0000 to 0x945F_FFFF

Offset	Description
0x00000	Interrupt status
0x00004	Interrupt enable
0x00008	MAC most significant address
0x0000C	MAC least significant address
0x00010	Multicast address table 0
0x00014	Multicast address table 1
0x00018	Transmit poll demand
0x0001C	Receive poll demand
0x00020	Transmit ring base address
0x00024	Receive ring base address
0x00028	Interrupt timer control
0x0002C	Automatic polling timer control
0x00030	DMA burst length and arbitration control
0x00034	MAC version
0x00038	Feature
0x0003C–0x00084	Reserved
0x00088	MAC control
0x0008C	MAC status
0x00090	PHY control
0x00094	PHY write data
0x00098	Flow control
0x0009C	Back pressure
0x000A0–0x000C0	Reserved
0x000C4	Test seed
0x000C8	DMA/FIFO state
0x000CC	Test mode
0x000D0	Reserved
0x000D4	TX_MCOL and TX_SCOL counter
0x000D8	RPF and AEP counter
0x000DC	XM and PG counter
0x000E0	RUNT_CNT and TLCC counter
0x000E4	CRCER_CNT and FTL_CNT counter
0x000E8	RLC and RCC counter
0x000EC	BROC counter
0x000F0	MULCA counter
0x000F4	RP counter
0x000F8	XP counter
0x000FC–0xFFFFC	Reserved

5.11.2 Timing

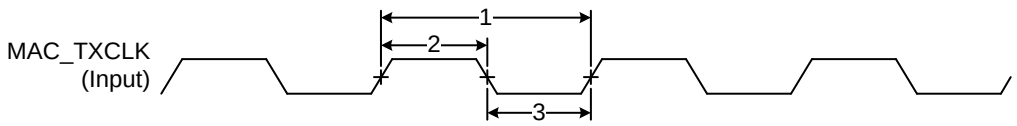


Figure 5–19 MAC_TXCLK Timing

Table 5–29 Timing Requirements for MAC_TXCLK

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{c(REF_CLK)}$	Cycle time, MAC_TXCLK	19.999	20.001	ns
2	$t_{w(REF_CLKH)}$	Pulse width, MAC_TXCLK high	7	13	ns
3	$t_{w(REF_CLKL)}$	Pulse width, MAC_TXCLK low	7	13	ns

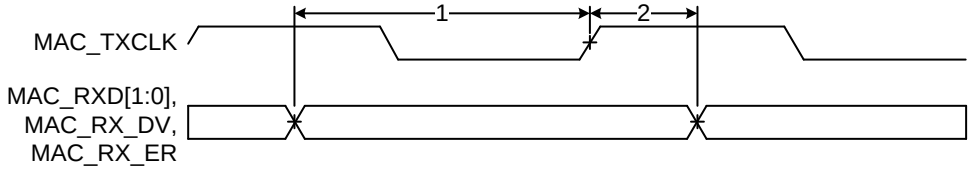


Figure 5–20 MAC_RXD[1:0], MAC_RX_DV, MAC_RX_ER Timing

Table 5–30 Timing Requirements for MAC_RXD[1:0], MAC_RX_DV, and MAC_RX_ER

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{su(RXD-REF_CLK)}$	Setup time, MAC_RXD[1:0] valid before REF_CLK	4	–	ns
	$t_{su(CRS_DV-REF_CLK)}$	Setup time, MAC_RX_DV valid before REF_CLK		–	ns
	$t_{su(RX_ER-REF_CLK)}$	Setup time, MAC_RX_ER valid before REF_CLK		–	ns
2	$t_{h(REF_CLK\ -RXD)}$	Hold time, MAC_RXD [1:0] valid after REF_CLK	2	–	ns
	$t_{h(REF_CLK\ -CRS_DV)}$	Hold time, MAC_RX_DV valid after REF_CLK		–	ns
	$t_{h(REF_CLK\ -RX_ER)}$	Hold time, MAC_RX_ER valid after REF_CLK		–	ns

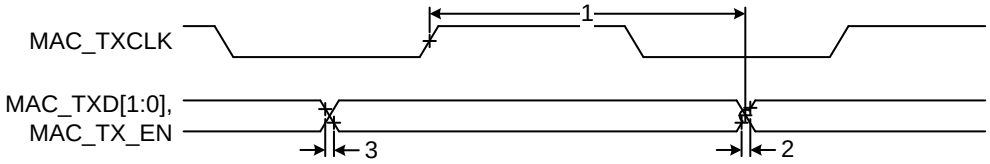


Figure 5–21 MAC_TXD[1:0], MAC_TX_EN Timing

Table 5–31 Switching Characteristics for MAC_TXD[1:0] and MAC_TX_EN

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{d(REF_CLK-TXD)}$	Delay time, REF_CLK high to MAC_TXD[1:0] valid	2	13	ns
	$t_{d(REF_CLK-TX_EN)}$	Delay time, REF_CLK to MAC_TX_EN valid			
2	$t_{r(TXD)}$	Rise time, MAC_TXD outputs	1	5	ns
	$t_{r(TX_EN)}$	Rise time, MAC_TX_EN output			
3	$t_{f(TXD)}$	Fall time, MAC_TXD outputs	1	5	ns
	$t_{f(TX_EN)}$	Fall time, MAC_TX_EN output			

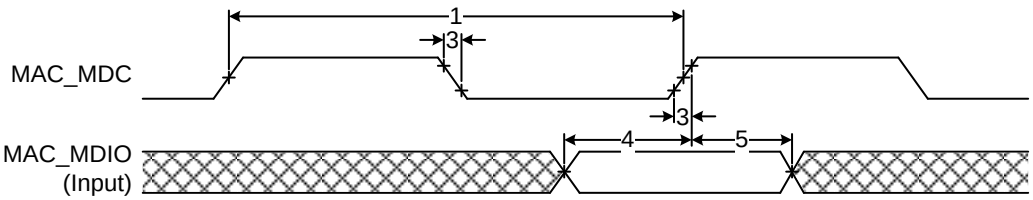


Figure 5–22 MDIO Input Timing

Table 5–32 Timing Requirements for Management Data Input/Output (MAC_MDIO)

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{c(MDC)}$	Cycle time, MAC_MDC	400	–	ns
2	$t_{w(MDC)}$	Pulse duration, MAC_MDC high/low	180	–	ns
3	$t_{t(MDC)}$	Transition time, MAC_MDC	–	5	ns
4	$t_{su(MDIO-MDCH)}$	Setup time, MAC_MDIO data input valid before MAC_MDC high	10	–	ns
5	$t_{h(MDCL-MDIO)}$	Hold time, MAC_MDIO data input valid after MAC_MDC high	0	–	ns

The table below lists switching characteristics over recommended operating conditions for MAC_MDIO output.

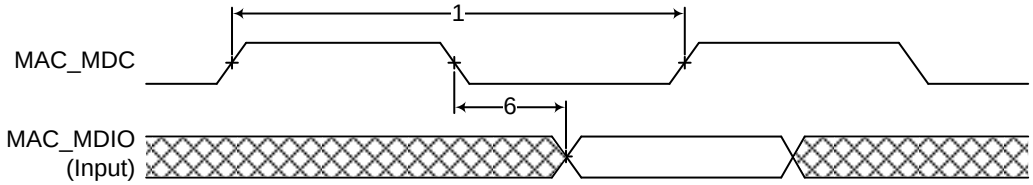


Figure 5–23 MAC_MDIO Output Timing

Table 5–33 Switching Characteristics for MAC_MDIO Output

No.	Parameter		Device		Unit
			MIN.	MAX.	
6	$t_{d(MDCL-MDIO)}$	Delay time, MAC_MDC low to MAC_MDIO data output valid	–	100	ns

5.12 Universal Serial Bus 2.0 (USB 2.0)

The SN93700 Series has two USB PHYs. The first USB PHY is dedicated for USB host, and the second is an alternative for a USB optional host or device.

Features of the USB 2.0 host include:

- Compliant to USB 2.0 specification
- Compliant to EHCI v0.96 specification
- Compliant to AMBA 2.0 specification
- Compliant to UTMI+ v1.0 specification
- USB 2.0 host all transfer modes (control, bulk, interrupt, and isochronous)
- One port for root hub function

– The companion host controller supports full-speed (FS) and low-speed (LS) functionalities, but it is not implemented based on OHCI or UHCI standard.
  ▪ Port router unnecessary-companion port route description for OHCI/UHCI
– Bus topology
  ▪ Only high-speed (HS) hub plugged into tier one layer
  ▪ Device only with HS control transfer/HS isochronous transfer/HS bulk transfer/ HS interrupt transfer plugged into the root hub
– Supports the following peripheral device types:
  ▪ USB mass storage (USB HD, pen drive, and USB DVD-RW)
  ▪ USB Wi-Fi dongle
  ▪ USB HS ISO video/audio
  ▪ USB HS hub
  ▪ USB HID device

Features of the USB 2.0 device include:

- Compliant to USB 2.0 specification
- Compliant to AMBA 2.0 specification
- HS and FS supported
- Control transfer supported by endpoint #0
- Two BULK-IN, one BULK-OUT, two ISO-IN, one ISO-OUT, and two INT-IN endpoints
- Scatter-gather DMA
- 6.5K bytes FIFO RAM shared by all endpoints
- Isochronous transfer type
- USB video class (UVC) bulk mode and isochronous mode
- USB audio class (UAC) isochronous mode
- Mass storage class (MSC)
- Human interface device (HID)

The USB 2.0 host **does not** support the following features:

- Split transaction isochronous transfer descriptor (siTD)
- Frame span traversal node (FSTN)
- OTG 2.0 specification (embedded host)
- Port power control (PPC)

5.12.1 USB 2.0 Host

The USB host includes a universal serial bus (USB) 2.0 host controller and a built-in USB 2.0 host PHY. Without the software intervention, the host controller can deal with a transaction-based data structure to offload some overheads from the CPU and automatically transmits/receives the data on the USB bus. The transceiver interface is UTMI + level 3, which supports the HS transfer with a HS hub. Lacking the siTD support, FS with isochronous transfer device cannot be applied to USB 2.0 host via a HS hub or root hub.

I. AHB Interface

The EHCI host controller (HC) is connected to the system by the AHB bus. The design requires both master and slave bus operations. As a master, the host controller is responsible for running cycles on the AHB bus to access transfer descriptors as well as transferring data between memory and the local data buffer. As a slave, the host controller monitors the cycles on the AHB bus and determines when to respond to these cycles. Configuration and non-real-time control access to the host controller operational registers are through the AHB bus slave interface.

II. EHCI Controller

The EHCI supports two transfer types: asynchronous and periodic. The periodic transfer type includes isochronous and interrupt, and the asynchronous transfer type includes control and bulk.

III. Interrupt Processing

HC-initiated communication with the host controller driver by interrupts. There are several events that may trigger an interrupt from the host controller. Each specific event sets a specific bit in the interrupt status register.

IV. DMA

The DMA is the central block in the data path. The DMA coordinates all access to the AHB master interface. There are two sources of bus mastering within host controller: the link list processor and the data buffer engine.

V. Data Buffer

The data buffer serves as the data interface between the AHB master and the USB protocol engine. It is a Ping-Pong FIFO RAM with 1024 bytes x 2 size.

VI. USB 1.1 Host Controller Interface

A new structure is created to substitute the OHCI/UHCI USB 1.1 control unit. The port routing logic was disregarded as there is only one port in root hub.

VII. Register Summary

Table 5–34 Register Summary of USB 2.0 Host

Address ranges: 0x9420_0000 to 0x942F_FFFF and 0x9430_0000 to 0x943F_FFFF

Offset	Description
0x00000	Capability register length and interface version number
0x00004	Structural parameters
0x00008	Capability parameters
0x00010	USB command
0x00014	USB status
0x00018	USB interrupt enable
0x0001C	USB frame index
0x00024	Frame list base address
0x00028	Current asynchronous list address
0x00054	Port status/control
0x00058–0xFFFFC	Reserved 🕮 **NOTE:** Should NOT be written. Writing any value to the reserved registers can cause unpredictable results.

VIII. Timing

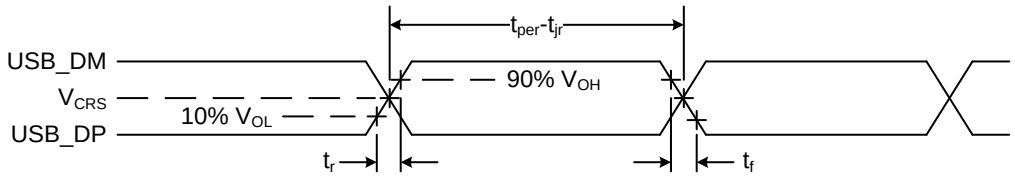


Figure 5–24 USB 2.0 Host Integrated Transceiver Interface Timing

Table 5–35 Switching Characteristics for USB 2.0 Host

Parameter		Device						Unit
		Low-Speed		Full-Speed		High-Speed		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{r(D)}$	Rise time, USB_DP and USB_DM signals[33]	75	300	4	20	0.5	20	ns
$t_{f(D)}$	Fall time, USB_DP and USB_DM signals[33]	75	300	4	20	0.5	20	ns
t_{frfm}	Rise/fall time, matching[34]	80	125	90	111.11	–	–	%
V_{CRS}	Output signal cross-over voltage[33]	1.3	2	1.3	2	–	–	V
$t_{jr(source)NT}$	Source (host) driver jitter, next transition	–	2	–	2	–	–	ns
$t_{jr(FUNC)NT}$	Function driver jitter, next transition	–	25	–	2	–	–	ns
$t_{jr(source)PT}$	Source (host) driver jitter, paired transition[35]	–	1	–	1	–	–	ns
$t_{jr(FUNC)PT}$	Function driver jitter, paired transition	–	10	–	1	–	–	ns
$t_{w(EOPT)}$	Pulse duration, EOP transmitter	1250	1500	160	175	–	–	ns
$t_{w(EOPR)}$	Pulse duration, EOP receiver	670	–	82	–	–	–	ns
$t_{(DRATE)}$	Data rate	–	1.5	–	12	–	480	Mb/s
Z_{DRV}	Driver output resistance	–	–	28	49.5	40.5	49.5	Ω

5.12.2 USB 2.0 Device

Other than a USB host, the SN93700 Series has a USB 2.0 high speed device interface, forward compatible with full speed mode. That enables the SN93700 Series to be a USB device supporting bulk, isochronous, interrupt, and control transfers that are compliant to the USB 2.0 specification.

The USB controller transfers data through the AHB bus and the USB bus. The AHB bus includes the AHB master interface and AHB slave interface. The CPU programs the USB controller through the AHB slave interface. For IN or OUT transfer, the USB controller writes data to system memory or reads data from system memory through the AHB master interface. The USB controller also includes a USB transceiver as interface of the USB.

USB endpoints: includes nine endpoints, designated EP0, EP1, EP3, EP4, EP5, EP7, EP12, EP13 and EP14. Each is intended for a particular use as below:

- EP0: the default endpoint uses control transfer (in/out) to handle configuration and control functions required by the USB specification.
- EP1: Interrupt in endpoint
- EP3: Isochronous in endpoint
- EP4: Isochronous out endpoint
- EP5: Interrupt in endpoint
- EP7: Isochronous in endpoint
- EP12: Bulk in endpoint
- EP13: Bulk out endpoint
- EP14: Bulk in endpoint

[33] Low Speed: CL = 200 pF, Full Speed: CL = 50 pF; High Speed: CL = 50 pF
[34] $t_{frfm} = (t_r / t_f) \times 100$; excluding the first transaction from the idle state
[35] $t_{jr} = t_{px(1)} - t_{px(0)}$

I. Register Summary

Table 5–36 Register Summary of USB 2.0 Device

Address ranges: 0x9440_0000 to 0x944F_FFFF

Offset	Description
0x00000	Global configuration
0x00004	Global status
0x00008	Global command
0x0000C	Isochronous Timestamp Packet (ITP)/Start Of Frame (SOF) number
0x00010	Reserved (Should not be written. Writing any value to the reserved registers can cause unpredictable results.)
0x00014	USB interrupt enable
0x00018	USB interrupt status
0x0001C	Endpoint select
0x00020	Endpoint transfer ring address
0x00024	Endpoint configuration
0x00028	Endpoint command
0x0002C	Endpoint status
0x00030	Reserved. (Should not be written. Writing any value to the reserved registers can cause unpredictable results.)
0x00034	Endpoint status enable
0x00038	Doorbell
0x0003C	Endpoint (EP) interrupt enable
0x00040	EP interrupt status
0x00044–0x00074	Reserved. (Should not be written. Writing any value to the reserved registers can cause unpredictable results.)
0x00078	Miscellaneous control
0x0007C–0xFFFFC	Reserved. (Should not be written. Writing any value to the reserved registers can cause unpredictable results.)

II. Timing

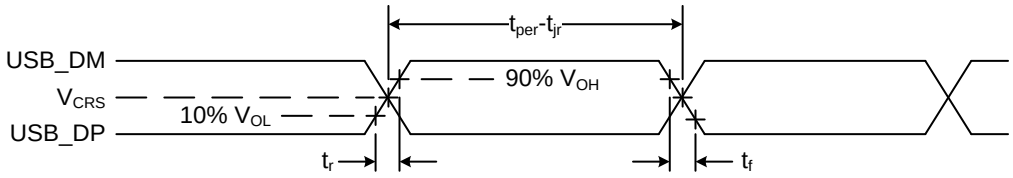


Figure 5–25 USB 2.0 Device Integrated Transceiver Interface Timing

Table 5–37 Switching Characteristics for USB 2.0 Device

Parameter		Full Speed		High Speed		Unit
		MIN.	MAX.	MIN.	MAX.	
$t_{r(D)}$	Rise time, USB_DP and USB_DM signals[33]	4	20	0.5	20	ns
$t_{f(D)}$	Fall time, USB_DP and USB_DM signals[33]	4	20	0.5	20	ns
t_{rfm}	Rise/fall time, matching[34]	90	111.11	–	–	%
V_{CRS}	Output signal cross-over voltage[33]	1.3	2	–	–	V
$t_{jr(source)NT}$	Source (host) driver jitter, next transition	–	2	–	–	ns
$t_{jr(FUNC)NT}$	Function driver jitter, next transition	–	2	–	–	ns
$t_{jr(source)PT}$	Source (host) driver jitter, paired transition[35]	–	1	–	–	ns
$t_{jr(FUNC)PT}$	Function driver jitter, paired transition	–	1	–	–	ns
$t_{w(EOPT)}$	Pulse duration, EOP transmitter	160	175	–	–	ns
$t_{w(EOPR)}$	Pulse duration, EOP receiver	82	–	–	–	ns

Parameter		Full Speed		High Speed		Unit
		MIN.	MAX.	MIN.	MAX.	
$t_{(DRATE)}$	Data rate	–	12	–	480	Mb/s
Z_{DRV}	Driver output resistance	28	49.5	40.5	49.5	Ω

5.13 Motor Controller (MC)

The motor controller provides two sets of four output signals for stepper motor control, and each set can be programmed independently. The motor controller is in base address, 0x9004_0000.

Features of the MC include:

- Two independent stepper motor controllers
- Programmable period
- Programmable high pulse duty
- Upper level pinmux options

5.13.1 Register Summary

Table 5–38 Register Summary of Motor Controller

Address ranges: 0x9004_0000 to 0x9004_FFFF

Offset	Description
0x00000	MT 0 mode
0x00004	Reserved
0x00008	MT 0 output and direction
0x0000C	MT 0 step counter
0x00010	MT 0 base time
0x00014	MT 0 period for one full step
0x00018	MT 0 high pulse time
0x0001C	Reserved
0x00020	MT 1 mode
0x00024	Reserved
0x00028	MT 1 output and direction
0x0002C	MT 1 step counter
0x00030	MT 1 base time
0x00034	MT 1 period for one full step
0x00038	MT 1 high pulse time
0x0003C	Clock bases for MT 0 and MT 1
0x00040–0x00FFFC	Reserved

5.13.2 Timing

The table below lists switching characteristics over recommended operating conditions for the MC.

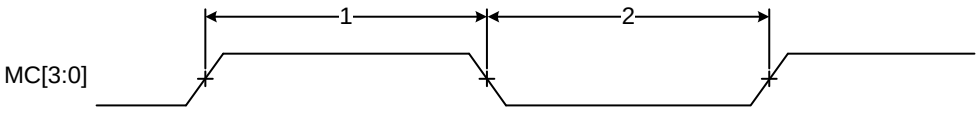


Figure 5–26 Motor Controller Timing

Table 5–39 Switching Characteristics for MC Outputs

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{w(MCOH)}$	Pulse duration, MC_[3:0] high	1 MT_CK12 cycle[36]	–	ns
2	$t_{w(MCOL)}$	Pulse duration, MC_[3:0] low	1 MT_CK12 cycle[36]	–	ns

5.14 Successive Approximation Register Analog-to-Digital Converter (SAR ADC)

SAR ADC has five channel inputs for battery detection, temperature sensors, key-scan input and general purpose.

Features of the SAR ADC include:

- Input 0–3.3V full swing
- Conversion rate up to 1M SPS
- Low latency-time
- Resolution (ENOB) > 9 bits
- Five channel inputs
- Upper level pinmux options

5.14.1 Register Summary

Table 5–40 Registers of SAR ADC

Address ranges: 0x9002_0000 to 9x9002_FFFF

Offset	Description
0x00000	SAR ADC enable
0x00004	Channel trigger to detect
0x00008	Channel ready
0x0000C0–0x00001C	Channel report
0x00020	SAR ADC control
0x00024–0x00FFFC	Reserved

5.14.2 Timing

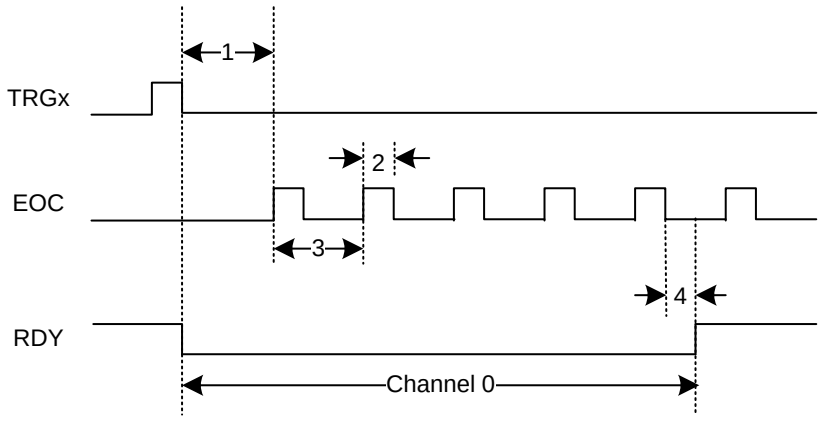


Figure 5–27 SAR ADC Channel 0 Timing Diagram

[36] *1 MT_CK12 cycle = MT_CK_BASE / 12 MHz*, MT_CK_BASE is at offset 0x3C in MC registers.

Table 5–41 Switching Characteristics for SAR ADC

No.	Parameter		Device		Unit
			MIN.	MAX.	
1	$t_{d(TRG_EOC)}$	Delay time, trigger to start EOC	2 T_{SAR_CLK}[37]	–	µs
2	$t_{w(EOC_CLKH)}$	Pulse duration, SAR sampled data valid EOC high	8 T_{SAR_CLK}[37]	–	µs
3	$t_{t(EOC_CLK)}$	Transition time, SAR sampled data valid EOC cycle	30 T_{SAR_CLK}[37]	–	µs
4	$t_{d(EOC_RDY)}$	Delay time, EOC low to RDY valid	0.167	–	µs

The time from trigger to sampled data ready is $t_{d(TRG_EOC)} + 4\,t_{t(EOC_CLK)} + t_{w(EOC_CLKH)} + t_{d(EOC_RDY)}$.

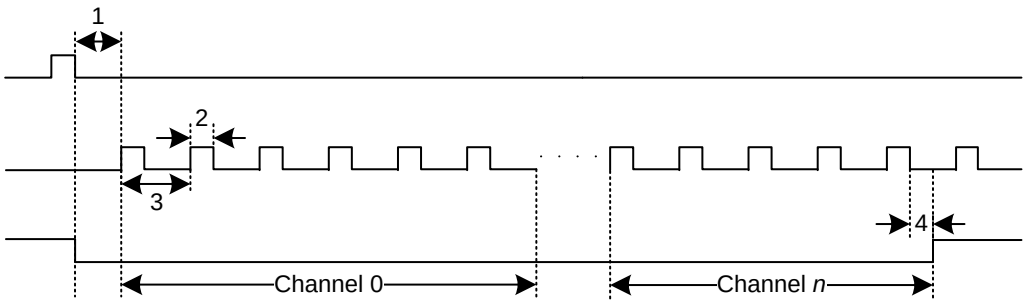


Figure 5–28 SAR ADC Single or Multi-Channel Timing

Examples of the time from trigger to sample data ready:

- Channel 0 + Channel 1 = $t_{d(TRG_EOC)} + 6\,t_{t(EOC_CLK)} + 4\,t_{t(EOC_CLK)} + t_{w(EOC_CLKH)} + t_{d(EOC_RDY)}$
- Channel 2 only = $t_{d(TRG_EOC)} + 6\,t_{t(EOC_CLK)} + 6\,t_{t(EOC_CLK)} + 4\,t_{t(EOC_CLK)} + t_{w(EOC_CLKH)} + t_{d(EOC_RDY)}$
- Channel 1 + Channel 2 = $t_{d(TRG_EOC)} + 6\,t_{t(EOC_CLK)} + 6\,t_{t(EOC_CLK)} + 4\,t_{t(EOC_CLK)} + t_{w(EOC_CLKH)} + t_{d(EOC_RDY)}$
- Channel 0 + Channel 3 = $t_{d(TRG_EOC)} + 3 \times 6\,t_{t(EOC_CLK)} + 4\,t_{t(EOC_CLK)} + t_{w(EOC_CLKH)} + t_{d(EOC_RDY)}$
- Channel 4 only = $t_{d(TRG_EOC)} + 4 \times 6\,t_{t(EOC_CLK)} + 4\,t_{t(EOC_CLK)} + t_{w(EOC_CLKH)} + t_{d(EOC_RDY)}$

5.15 RF Serial Peripheral Interface Bus (SPI)

RF_SPI is a SONiX proprietary SPI controller with RF module. Controlling the RF module with RF_SPI SDK optimizes the transmission with new algorithm and avoids interference for devices to coexist in 2.4 GHz band.

Features of the RF_SPI include:

- Two sets of SPI controller with RF module
- Supports 2.4 GHz ISM-Band RF transceivers including AMICCOM A7130 (4 Mbps) and AMICCOM A7196 (6 Mbps)
- Firmware protocol base adaptive Frequency-hopping Spreading Spectrum (FHSS)
- Firmware protocol for anti-interference algorithm
- ID paring for security

[37] *SAR_CLK = (2 x SAR_RATE) / 6 MHz*

6 Device Operating Conditions

6.1 Absolute Maximum Ranges
6.2 Recommended Operating Conditions
6.3 AC Characteristics
6.4 Power-up and Power-down Sequence

6.1 Absolute Maximum Ratings

Table 6–1 Absolute Maximum Ratings[38] [39]

Parameter		Rating	Unit
Supply Voltage Ranges	All 1.20V supplies	-0.30 to 1.26	V
	All 1.80V supplies	-0.30 to 1.90	
	All 2.50V supplies	-0.30 to 2.75	
	All 3.30V supplies	-0.30 to 3.60	
Input Voltage Ranges	All 1.80V I/Os	-0.30 to 1.90	
	All 3.30V I/Os	-0.30 to 3.60	
Ambient Temperature Ranges (T_A)		0 to 70	°C
Operating Junction Temperature Ranges (T_J)		0 to 125	
Storage Temperature Ranges (T_{STG})		-40 to 150	
Junction-to-ambient Thermal Resistance (θ_{JA})		31.063	°C/W

6.2 Recommended Operating Conditions

Table 6–2 Recommended Operating Conditions

Name	Description	MIN.	TYP.	MAX.	Unit
Crystal Clock					
XIN	System clock except RTC frequency	–	12	–	MHz
RTC XIN	RTC clock frequency	–	32768	–	Hz
Supply Voltage					
VDD	1.2V core supply voltage	1.14	1.20	1.26	V
VDD_MIPI	1.2V MIPI supply voltage	1.14	1.20	1.26	V
VDDSSTL	1.2V DDR2 supply voltage	1.14	1.20	1.26	V
DEV_VDDL1	1.2V DEV supply voltage	1.14	1.20	1.26	V
HOST_VDDL1	1.2V USB 2.0 PHY supply voltage	1.14	1.20	1.26	V
VDDIO_SEN33/18	1.8V sensor I/O supply voltage	1.7	1.8	1.9	V
	3.3V sensor I/O supply voltage	3.0	3.3	3.6	V
VDDPSSTL (V_{DDQ})	1.8V DDR2 supply voltage	1.7	1.8	1.9	V
VREFSSTL (V_{REF})	DDR2 reference supply voltage Condition: 0.5 x VDDPSSTL	0.85	0.9	0.95	V
EFUSE_VDDQ	Electrical fuse supply voltage at normal mode	–	0	–	V
DEV_VDDD1	3.3V DEV supply voltage	3.0	3.3	3.6	V
VDD33	3.3V I/O supply voltage	3.0	3.3	3.6	V
DAC_VDDA	3.3V R2R DAC supply voltage	3.0	3.3	3.6	V
ADC_VDDA	3.3V ADC supply voltage	2.3	3.3	3.6	V
RTC_VDDIO	3.3V RTC supply voltage	1.4	3.3	3.6	V
HOST_VDDD1	3.3V USB 2.0 PHY supply voltage	3.0	3.3	3.6	V
Supply Ground					
Thermal pad	3.3V I/O ground	0	0	0	V
	1.2V core ground	0	0	0	V

[38] Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if the operation exceeds the maximum ratings.
[39] All voltage values are with respect to VSS.

Name	Description	MIN.	TYP.	MAX.	Unit
	1.8V DDR2 ground	0	0	0	V
	1.2V DDR2 ground	0	0	0	V
	3.3V R2R DAC I/O ground	0	0	0	V
	3.3V ADC I/O ground	0	0	0	V
	USB 2.0 PHY ground	0	0	0	V
DAC_GNDA	3.3V R2R DAC ground	0	0	0	V
ADC_GNDA	3.3V ADC ground	0	0	0	V

Table 6–3 Electrical Characteristics over Recommended Ranges

Parameter		Conditions	MIN.	TYP.	MAX.	Unit
Input Voltage	V_{IL}	–	-0.30	–	0.80	V
	V_{IH}	–	2.00	–	3.60	V
Output Voltage	V_{OL}	–	–	–	–	–
		–	–	–	0.40	V
	V_{OH}	–	2.40	–	–	V
	I_{OL_8mA}	V_{OL} = 0.40V	12.7	19.3	25.9	mA
	I_{OL_12mA}	V_{OL} = 0.40V	16.9	25.6	34.1	mA
	I_{OL_16mA}	V_{OL} = 0.40V	21.0	31.9	42.5	mA
	I_{OH_8mA}	V_{OH} = 2.40V	18.7	37.0	62.8	mA
	I_{OH_12mA}	V_{OH} = 2.40V	24.0	47.5	80.5	mA
	I_{OH_16mA}	V_{OH} = 2.40V	32.0	63.2	107.1	mA
Input Capacitance	C_i	–	–	2.9	–	pF
Output Capacitance	C_o	–	–	2.9	–	pF
Internal pull-down resistance	R_{PD}	–	52K	78K	128K	Ω

6.3 AC Characteristics

Table 6–4 AC Value Summary

Title	See
Switching Characteristics for LCD Controller in CPU Mode	Table 4–5
Switching Characteristics for LCD Controller in Non-CPU Mode	Table 4–6
Switching Characteristics for I2S Master Transmitter	Table 4–7
Switching Characteristics for I2S Slave Transmitter	Table 4–9
Switching Characteristics for I2S Master Receiver	Table 4–10
Switching Characteristics for GPIO Outputs	Table 5–3
Switching Characteristics for I²C	Table 5–6
Switching Characteristics for PWM Outputs	Table 5–8
Switching Characteristics for SPI in Master Mode	Table 5–10
Switching Characteristics for SPI in Slave Mode	Table 5–12
Output Switching Characteristics of 4-pin Chip-select Option in Master Mode	Table 5–14
Output Switching Characteristics of 4-pin Chip-select Option in Slave Mode	Table 5–15
Switching Characteristics for UART Transmitter	Table 5–19
Switching Characteristics for SF Controller	Table 5–21
Switching Characteristics for JTAG Test Port	Table 5–24
Switching Characteristics for MAC_TXD[1:0] and MAC_TX_EN	Table 5–31
Switching Characteristics for MAC_MDIO Output	Table 5–33
Switching Characteristics for USB 2.0 Host	Table 5–35
Switching Characteristics for USB 2.0 Device	Table 5–37
Switching Characteristics for MC Outputs	Table 5–39
Switching Characteristics for SAR ADC	Table 5–41

6.4 Power-up and Power-down Sequence

6.4.1 Power-up Sequence

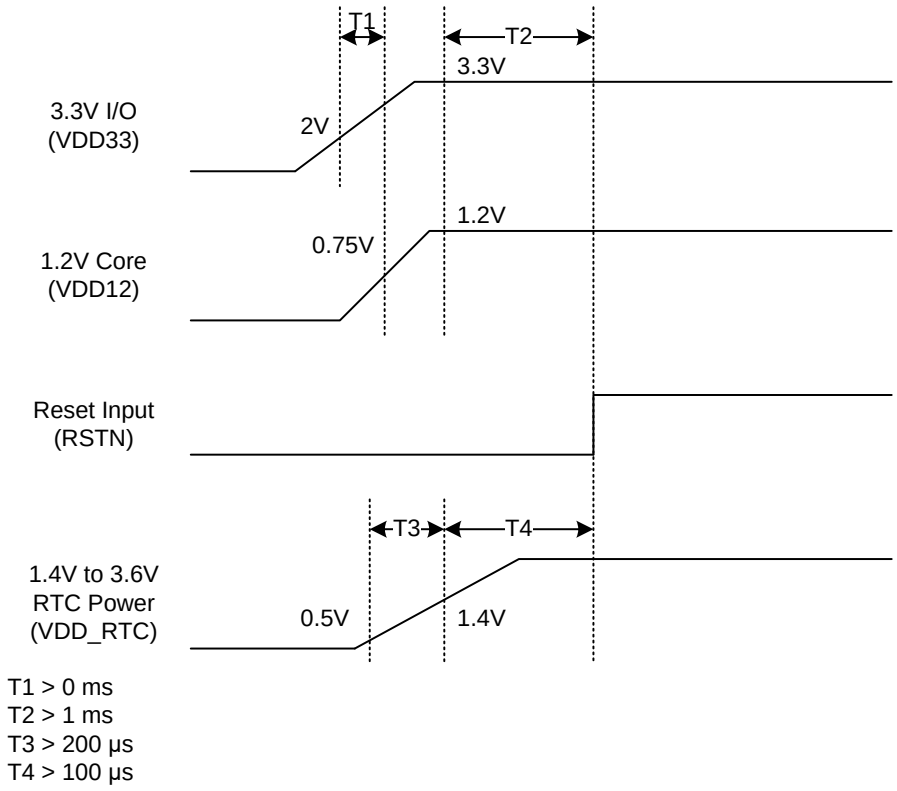


Figure 6–1 Power-up Sequence

Designs of the SN93700 Series must comply with the power-up sequence guidelines below to ensure reliable operation of the device.

STEP 1: Turn on the VDD33 for I/O power.

STEP 2: Turn on the VDD12 for core power.

🕮 NOTE	The power-on circuit is active for power-on-reset when VDD33 > 2V and VDD12 < 0.75V.

STEP 3: Release/pull up the reset pin (RSTN) after all power voltages are stable, and the time is greater than 1 ms (T2).

Requirements:

- The slew rate of VDD_RTC voltage needs to be more than 200 µs from 0.5V to 1.4V as T3 in the figure above.
- The VDD_RTC[40] must be over 1.4V before releasing RSTN while the time is greater than 100 µs as T4 in the figure above.

6.4.2 Power-down Sequence

The power-down sequence does not have any special requirements.

[40] VDD_RTC can be ignored when RTC is not used.

7 Mechanical Data

7.1 Thermal Data
7.2 Package Information
7.3 Packaging Appearance and Storage Information

7.1 Thermal Data

The permissible operating temperature range for the bearing is 0 °C to 70 °C.

7.2 Package Information

7.2.1 Nomenclature

LOGO
Product ID
DATECODE + (SONIX) + e3 (Eco-friendly Products)

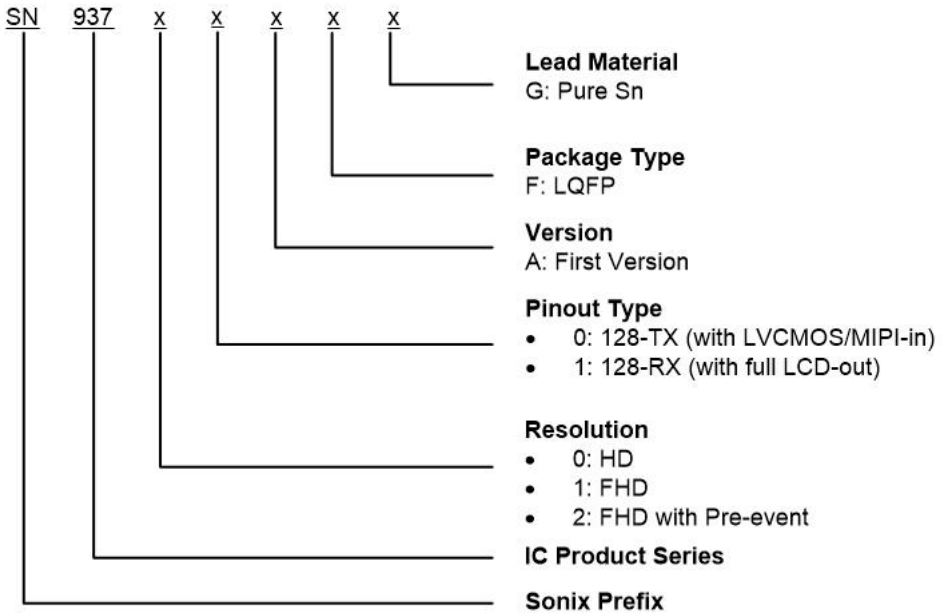
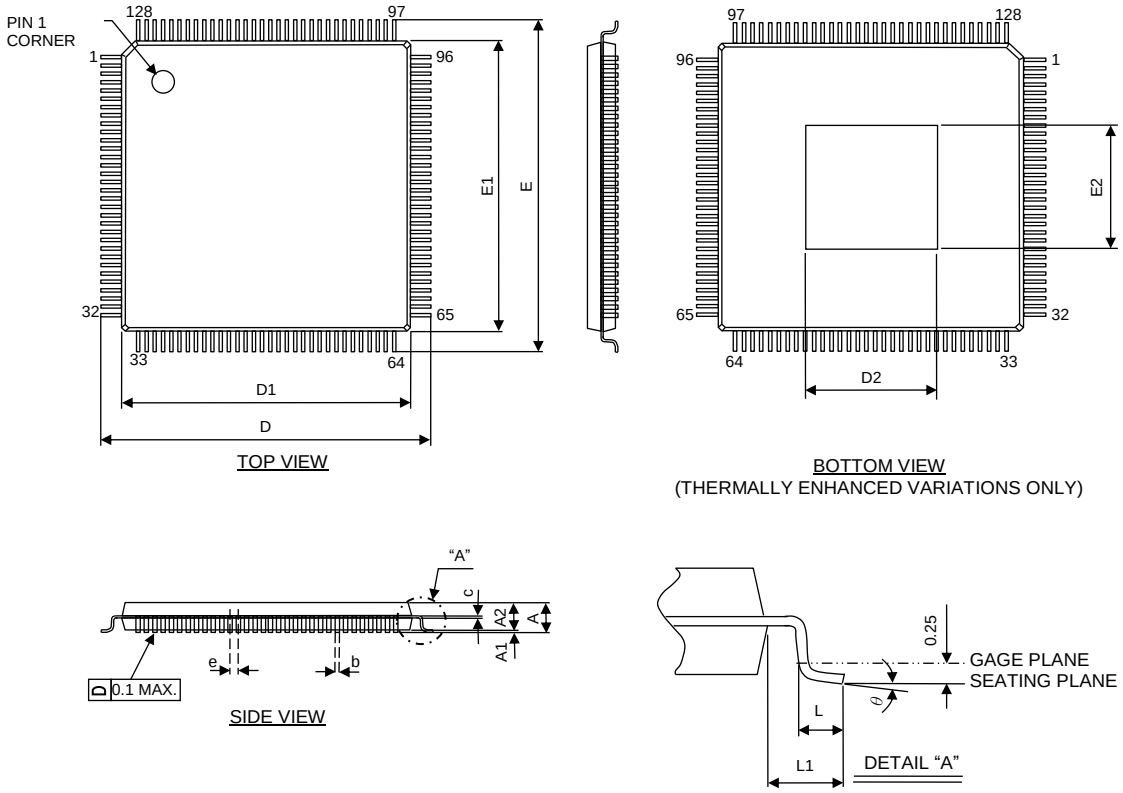


Figure 7–1 Device Nomenclature

7.2.2 Package Dimensions



Symbols	Dimension in mm[41]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b[42]	0.13	0.18	0.23	0.005	0.007	0.009
c	0.09	–	0.20	0.004	–	0.008
D	16.00 BSC			0.630 BSC		
D1[43]	14.00 BSC			0.551 BSC		
E	16.00 BSC			0.630 BSC		
E1[43]	14.00 BSC			0.551 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
θ	0˚	3.5˚	7˚	0˚	3.5˚	7˚
Thermal Enhanced Dimensions						
D2	5.10	6.25	7.40	0.201	0.246	0.291
E2	5.10	6.25	7.40	0.201	0.246	0.291

[41] Controlling dimension: millimeter (mm)
[42] Dimension b does not include dambar protrusion.
[43] Dimension D1 and E1 do not include mold protrusion.

7.3 Packaging Appearance and Storage Information

7.3.1 Packing Quantity Information

Table 7–1 Packing Quantity Information

Type	Pin Count	Carry Type	Package Size	IC Q'ty per Tube or Tray or Reel	Tube or Tray or Reel Q'ty per Inner Box	Total Q'ty in One Inner Box	Inner Box Q'ty per Carton	IC Q'ty per Carton
LQFP	128	Tray	14 x 14	90	10	900	6	5400

7.3.2 Packing Box/Carton Dimension

Table 7–2 Packing Box/Carton Dimension

Inner Box/Carton	Dimension in mm
Inner Box	360 x 152 x 90
Carton	470 x 370 x 210
Carton (option)	380 x 340 x 300

7.3.3 Temperature and Humidity Environmental Control Requirements in Storage

Table 7–3 Store Condition

Control Requirement	Specification
Temp (°C)	24 ± 6
Humid. (%RH)	60 ± 20

7.3.4 Shelf-life

1. The shelf life for unopened vacuum pack products is four years after the date on the label.
2. Once the packaging is opened the product should be conducted SMT process within 168 hours and environmental control is under ≤ 30 °C / 60 %RH.
3. If the product has been exposed to the room environment for more than 168 hours, it should be baked in an oven at 125 °C for 10 hours and vacuum packed.

Appendix A – The SN93700 Series SDK

Description

The SDK structure includes three layers, application layer, middleware layer and driver layer. Figure A1 shows the components and structures of all layers.

Please note that all libraries and the RTOS itself in RTOS SDK are static.

For complete details on the SN93700 Series SDK, contact the nearest SONiX field sales office or an authorized distributor.

SDK Architecture

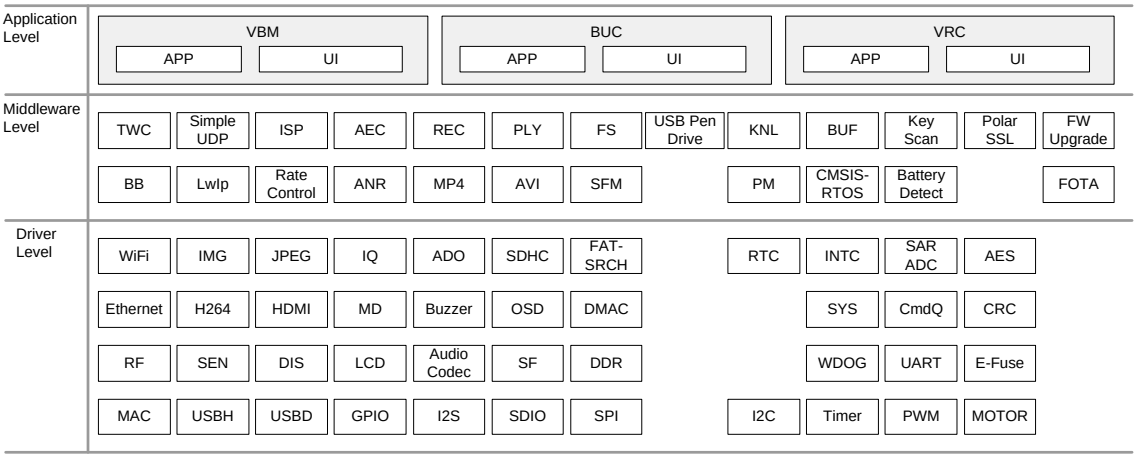


Figure A1 SDK Structure Based on RTOS for SN93700 Series

TERMS AND CONDITIONS

1. Content: Sonix Technology Co. Ltd. ("Sonix") provides the information in this Data Sheet as a convenient reference for its customers who use its products. While Sonix takes care to prepare this information, it may contain typographical errors or outdated technical information as Sonix will continue to update its integrated chip products with enhancements, improvements and other changes to better serve the needs of its customers. This Data Sheet covers products offered in Taiwan and may not reflect the products offered in other countries. Users of this Data Sheet should inquire of the appropriate Sonix representative to obtain the latest relevant information concerning the product(s) in question before placing their order. All Sonix's products are sold subject to Sonix's terms and conditions of sale that are supplied at the time of order.

2. No Warranty: The information contained herein is presented only as a reference for product use. Unless expressly set forth otherwise, Sonix does not warrant or represent that any license, either express or implied, is granted by this Data Sheet relating to any combination, machine, or process in which Sonix products are used (or to be used). Information in this Data Sheet regarding third-party products is not a license for use of such products, or a warranty or endorsement thereof. No license to any intellectual property is granted by this document, whether express or implied, by estoppel or otherwise. Absent a written signed agreement or except as provided in the relevant terms and conditions of sale for the products, and to the maximum extent allowable by law, (1) SONIX ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION, AND LOSS OF DATA, AND (2) SONIX DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.

3. Customers' Use: SONIX ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGNS OR APPLICATIONS of the products covered by the Data Sheet. While from time to time Sonix may be asked to assist users of its products, Sonix assumes no liability for assistance with, or the design of, users' own application of Sonix's products, including but not limited to: (a) determining the appropriateness of the use of Sonix products in the desired design or application; (b) evaluating and determining the applicability of any information contained in this Data Sheet, or in charts, diagrams, programs, algorithms, sample application circuits, or other referenced documents; and (c) validating all operating parameters for such designs and applications. Finally, Sonix products shall not be used for, or incorporated into, any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.

4. Improper & Unintended Use: SONIX'S PRODUCTS ARE NOT INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY OR RELIABILITY, OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE, OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE"). Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the military or aerospace industry, medical equipment, equipment used for automobiles, trains, ships, and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators, and escalators, devices related to electric power, and equipment used in finance-related fields. Further, only those products that Sonix has specifically designated as "military grade" are designed and intended for use in military or aerospace applications or environments. Users acknowledge and agree that any military or aerospace use of Sonix products that have not been so designated is solely at the user's risk, and that the user is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

SONiX Technology

Headquarter
10F-1, No.36, Taiyuan Street,
Zhubei City, Hsinchu, Taiwan
Tel: +886-3-5600-888
Fax: +886-3-5600-889
http://www.sonix.com.tw/masterpage-en

Taipei Office
15F-2, No.171, Song Ted Road,
Taipei, Taiwan
Tel: +886-2-2759-1980
Fax: +886-2-2759-8180
mkt@sonix.com.tw | sales@sonix.com.tw

Japan Office
Kobayashi bldg. 2F, 4-8-27, Kudanminami,
Chiyodaku, Tokyo,
102-0074, Japan
Tel: +81-3-6272-6070
Fax: +81-3-6272-6165
jpsales@sonix.com.tw

Hong Kong Office
Unit 2603, 26/F CCT Telecom Building,
No. 11, Wo Shing Street, Fo Tan,
New Territories, Hong Kong
Tel: +852-2723-8086
Fax: +852-2723-9179
hk@sonix.com.tw

Shenzhen Office
High Tech Industrial Park,
Shenzhen, China
Tel: +86-755-2671-9666
Fax: +86-755-2671-9786
mkt@sonix.com.tw | sales@sonix.com.tw

Chengdu Office
Tian Fu Software Park,
Cheng Du City, China
Tel: +86-28-8533-1818
Fax: +86-28-8533-1816
mkt@sonix.com.tw | sales@sonix.com.tw

United States Representative
Tim Lightbody
Tel: +1-714-330-9877
usa@sonix.com.tw